the application of linear microcircuits
volume 1

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THE APPLICATION OF LINEAR MICROCIRCUITS

by
the Applications Engineering Staff of SGS

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1. INTRODUCTION

1.1 PURPOSE OF HANDBOOK

This Handbook has been produced so as to bring under one cover as much information as possible likely to be of use to Systems and Electronic Design engineers who are contemplating using linear integrated circuits from the SGS family to solve their specific circuit problems.

Where possible, practical circuits have been included with actual component values but, due to the many applications that are possible, supplementary notes are included, giving explanations for the design values. By this means, and with the additional information available under the more general headings of Frequency Compensation, Noise, Power Supplies etc., it is hoped that the engineer will be in a position to adapt these circuits to his own requirements.

The Sections on basic amplifier circuits have been added for the benefit of engineers newly entering the field of operational amplifier usage.

1.2 INSTRUCTIONS FOR HANDBOOK USAGE

It will be noted that the contents are divided into Sections and sub-Sections which are identified by means of a two or three digit code.

The location of any the specified material shown in the « List of Contents » pages can therefore be readily found. The date of issue is indicated at the foot of the second page.

The Company should be consulted to obtain the latest information available concerning the Linear Integrated Circuit family.

Unless otherwise specifically stated, the pin numbers shown in various circuit diagrams refer to the TO-5 package. For the connections applicable to other alternative packages, the appropriate data sheet should be consulted.

1.3 ECONOMICS OF INTEGRATED CIRCUITS COMPARED WITH DISCRETE-COMPONENT CIRCUITS

The technical advantages of integrated circuits are discussed in Section 2.1, but it is of interest to consider in general terms the economic factors which may affect the choice of whether integrated circuits are adopted for a particular design or not.

In the past, integrated circuits have been used mainly in designs where the prime concern was only to save weight or space. The additional bonus of reduced power consumption and extra reliability may have been of secondary importance. In these circumstances, the cost factor was not necessarily considered.

With improvements in the techniques for fabrication of integrated circuits, resulting in higher yields and a steady reduction in price and also because new circuit designs are becoming available with a wider choice of operations with increasingly better performance, it is now possible to build up many systems where much of the electronics can be provided equally well by integrated circuits or discrete components. The choice in this case becomes an economic one.

Fig. 1.1 is a simple diagrammatic representation of how the individual steps in manufacture of a piece of electronic equipment contribute to the total cost. Although both the circuit problems themselves and the internal organisation of the manufacturer building the equipment vary enormously, in very general terms it can be shown that, with the possible exception of item (a), the cost of each stage is reduced to some degree by adopting integrated circuits.

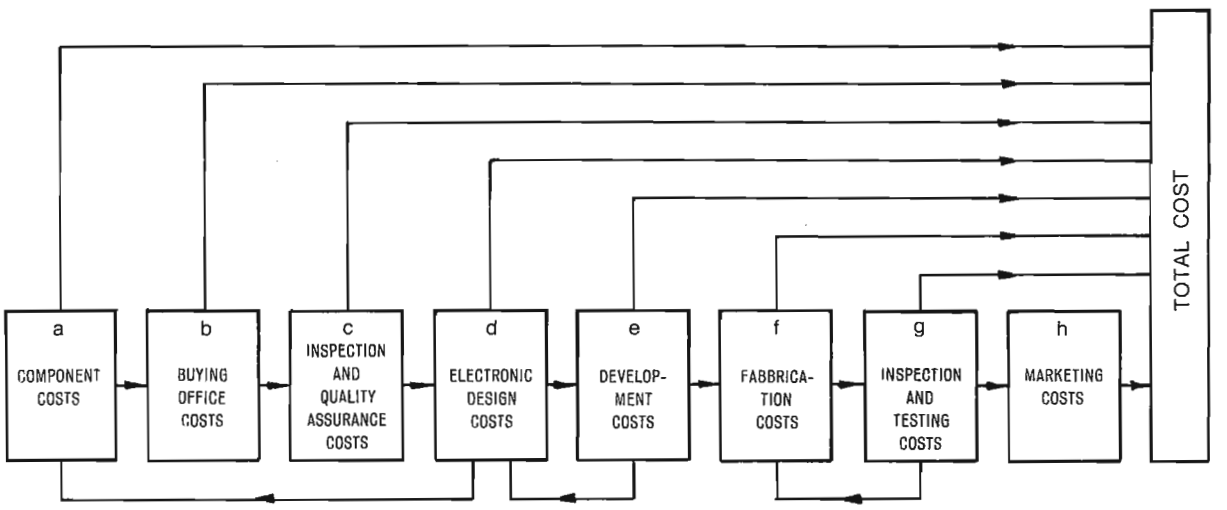


Fig. 1.1 - Schematic of Total Equipment Cost Breakdown

COMPONENT COSTS

The cost of the individual item necessary to make a discrete-component Linear Circuit equivalent in performance to an Integrated Circuit is often more than the total cost of the integrated circuit itself. This is due to the relatively high cost of matched transistors and high-stability resistors usually required in this type of circuit.

BUYING OFFICE COSTS

It is obvious that the organisation necessary to co-ordinate the purchase of quantities of individual components from a variety of manufacturers is comparatively costly, leaving aside the possibility of delayed delivery and its consequences on the production programme.

INSPECTION AND QUALITY ASSURANCE

Here again, the costs attached to handling and testing a number of items is very heavy compared to that of an individual integrated circuit.

ELECTRONIC DESIGN COSTS

In the design of both simple and complex systems, the overall man-hours spent on pure design are drastically reduced since integrated circuits can

provide guaranteed performances for well-defined circuit operations and environmental ranges.

DEVELOPMENT COSTS

These are likely to be greatly reduced as well, for the same reasons that extensive development has already been carried out on the complete integrated circuit by the manufacturer, with the result that system performance can be more accurately predicted at the « paper work » stage. The necessity for circuit modification, which is always a difficult and costly procedure once production has started, is thus reduced to a minimum. In general, it is also often easier to carry out where integrated circuits have been used.

FABRICATION COSTS

Considerable saving in labour costs can be achieved by adopting integrated circuits. Both the materials (tag boards, sockets, heat-sinks, etc.) and the assembly time can be very much reduced. At the time of writing, an increasing number of manufacturers are offering low cost mounting facilities specifically designed for integrated circuits, with flexible interconnection system. The range of alternative packages offered by SGS, combined with a standardised mounting system adopted by a specific manufacturer, minimises the necessity for costly « one off » configurations. Systems containing many repetitive circuits have abvious additional advantages.

INSPECTION AND TESTING COSTS

At all levels this should be reduced, both because performance of integrated circuits is more predictable and parameter tolerances may be « designed out » at the initial stages and because interconnections, both soldered and by plug and socket, can be decimated. Analysis of system reliability shows that interconnection failures contribute significantly to the overall probability of system failure where discrete components are used.

MARKETING

The utilisation of integrated circuits has reached a stage when the more sophisticated customer of an equipment manufacturer is beginning to expect the supplier to be incorporating integrated circuits in his designs.

In much the same way as, ten years ago, people were pointing out the advantages, of transistorisation so, today, integrated circuits are shown to be the next logical step forward.

The incorporation of integrated circuits manufactured by a Company whose reputation for performance and reliability is already well established can only help to increase confidence in the finished product.

2. DESIGNS FOR MONOLITHIC LINEAR INTEGRATED CIRCUITS

2.1 DESIGN PHILOSOPHY

2.1.1 Integrated Circuits Compared with Discrete Components

The design of complete circuits (e.g. high-gain, general-purpose amplifiers), which are to be realised as integrated circuits rather than made up from separate components, requires a new concept in the basic approach. This is due not only to certain limitations inherent in integrated manufacturing techniques but also because of new design freedoms that it allows.

In general, it is true to say that the total cost of a discrete component circuit is directly proportional to the number of transistors, capacitors and resistors in descending order of importance. PNP or NPN transistors may be used at will, but matching of separate transistors for gain, V_{BE}, etc., incurs considerable cost penalties while the necessity for specifying certain resistor values to close tolerance does not have the same significance.

With integrated circuits, it is possible to diffuse in both NPN and PNP devices, but for ease of manufacture, it is generally preferred to keep to NPN exclusively, for the more simple circuits. With integrated circuits there is more freedom in the number of active three-layer or two-layer junctions wich may be used. This is because doubling the number of such junctions (with the proviso that no extra processes are involved and that the overall yield is not significantly reduced) will certainly not increase the cost proportionally. Existing techniques by which resistors are formed makes it impractical to guarantee their absolute value to closer than 20% of nominal. It is possible, however, to achieve tolerances of better than 5% in the ratio between two resistors of the same value, by ensuring that they are placed in close physical proximity to each other and have identical layouts. Extra width in resistor track also reduces relative masking errors.

Compared with high-stability resistors, the temperature coefficient of semiconductor resistors is high (typically 0.2% per degree Centigrade). When resistor value ratios are important they should be kept at a maximum distance from potential sources of thermal dissipation and in any case should have a geometric axis of mutual symmetry which is at right angles to isothermal lines caused by such sources. Having the resistors close to each other reduces thermal resistance between them and therefore minimises differential changes in resistance caused by self-heating.

The fabrication of capacitors and even inductors of very small value, suitable for VHF are feasible but result in considerable complications in manufacture and are therefore to be avoided in design if possible. Diodes and Zeners of a generally fixed nominal value (approximately 6 V) are available at small cost by making use of the forward and reverse characteristics of a PN diffused layer where appropriate. Reduced dynamic impedance for the Zener may be obtained by using a transistor in a diode configuration.

It may be seen, therefore, that the design philosophy for integrated amplifiers is based on essentially symmetrical circuits, where possible, with inherent

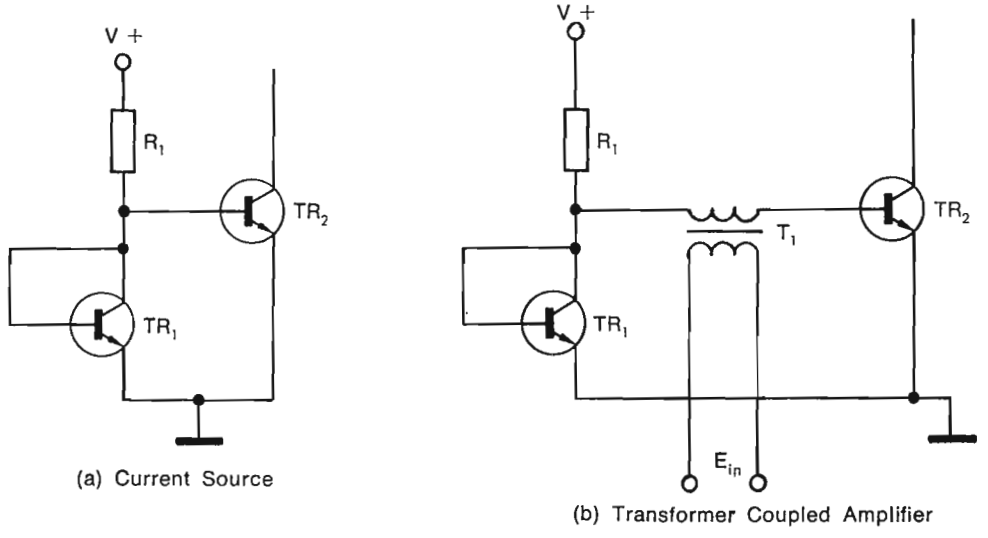


Fig. 2.1 - Biasing Techniques Applicable to Integrated Circuits which take advantage of Precise Matching and Close Thermal Coupling

immunity from drift caused by absolute resistor value changes.

D.C. coupling between stages should be used to eliminate capacitors. Offset voltage is minimised by a differential input stage. V_{BE} and its associated temperature coefficient is controlled by careful diffusion and the physical geometry of the transistor junctions which have their dimensions matched to the current being handled.

2.1.2 Integrated Circuit Solutions for Obtaining Specific Circuit Functions

(A) BIASING CIRCUITS

One of the most basic problems encountered in integrated circuits is bias stabilization of a common-emitter amplifier. Conventional methods usually require substantial D.C. degeneration and bypass capacitor to reduce the degeneration at the frequencies to be amplified. With integrated circuits, the required bypass capacitors are much too large to be practical. In the past, this problem has been overcome using some sort of differential or emitter-coupled amplifier connection. These solutions have been adequate in many instances but suffer from a lack of versatility.

The close matching of components and tight thermal coupling obtained in integrated circuits permit much more radical solutions. An example is given in Fig. 2.1 (a).

A current source can be implemented by imposing the emitter-base voltage of a diode-connected transistor operating at one collector current across the emitter-base junction of a second transistor.

If the two transistors are identical, the collector currents will be equal; hence, the operating current of the current source can be determined from the resistor (R_1) and the supply voltage (V+). Experiment has shown that this biasing scheme is stable over a wide temperature range even for power dissipations in TR_2 above 100 mW.

An extension of this idea is shown in Fig. 2.1 (b). A transformer with a low-resistance secondary can be inserted between the biasing transistor (TR_1) and the second transistor (TR_2). Then TR_2 is stably biased as an amplifier without requiring any bypass elements and the transformer secondary is coupled to the amplifier without disturbing the bias conditions.

A third and more subtle variation is given in Fig. 2.2.

If R_3 and R_4 as well as TR_1 and TR_2 are identical, the collector currents of the two transistors will be equal since their bases are driven from a common voltage point through equal resistances. The collector current of TR_1 will be given by

$$I_{C1} = \frac{V^+ - V_{BE}}{R_1} - \left(2 + \frac{R_3}{R_1}\right) I_B \quad \ldots\ldots\ldots\ldots\ldots (1)$$

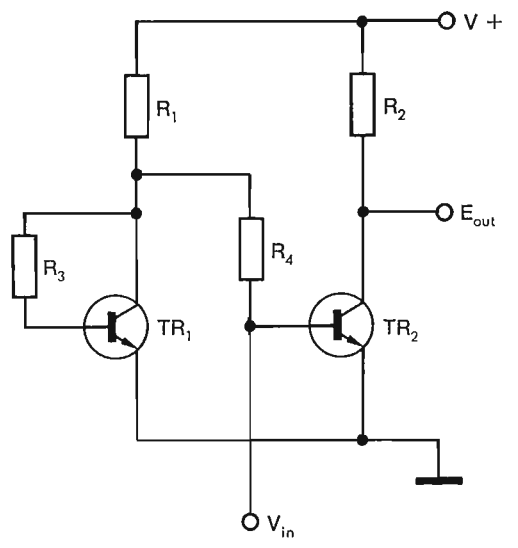


Fig. 2.2 - R.C. Coupled Amplifier

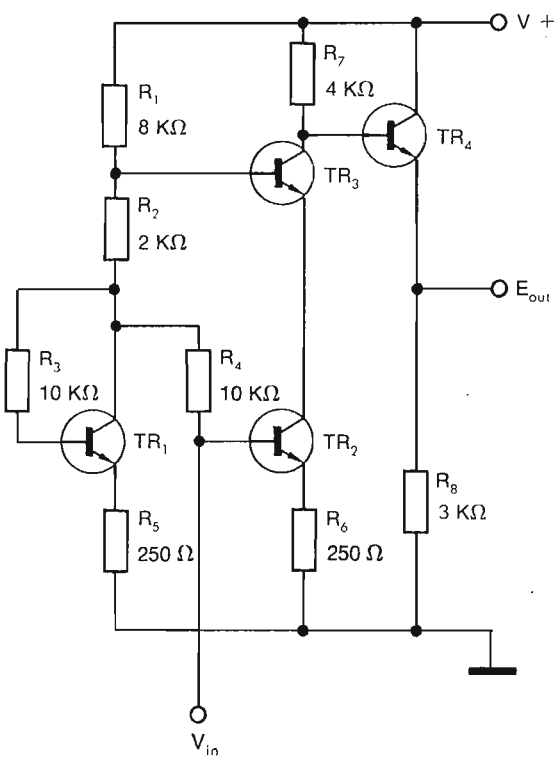


Fig. 2.3 General Purpose Wideband Amplifier using Balanced Biasing Techniques

where a single V_{BE} and I_B term is used since both transistors are identical. For

$$V_{BE} \ll V^+ \text{ and } \left(2 + \frac{R_3}{R_1}\right) I_B \ll I_{C1}$$

$$I_{C1} = I_{C2} \approx \frac{V^-}{R_1} \qquad \ldots\ldots\ldots\ldots\ldots\ldots (2)$$

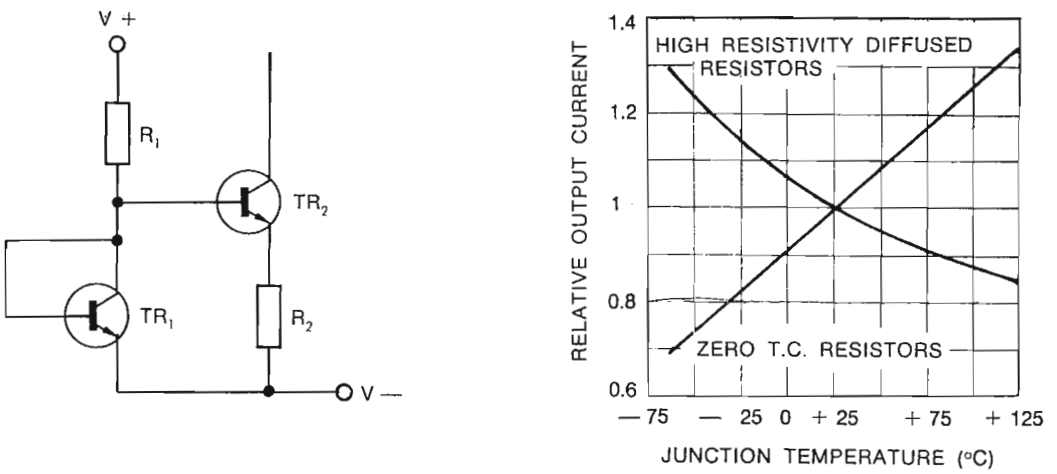
$$\text{If } R_2 = \frac{1}{2} R_1, \text{ then } E_o \approx \frac{V^+}{2} \qquad \ldots\ldots\ldots\ldots\ldots (3)$$

which means that the amplifier will be biased at its optimum operating point, at one-half the supply voltage, independent of the supply voltages as well as temperature and dependent only on how well the parts within the integrated circuit match.

A simple amplifier using the biasing of Fig. 2.2 is illustrated in Fig. 2.3. An emitter degeneration resistor (R_6) is employed in conjunction with R_5 to control gain and raise input impedance without disturbing the balance biasing. A cascode connection of TR_2 with TR_3 reduces input capacitance while the emitter-follower (TR_4) gives a low output impedance.

It can be seen from the above that the matching characteristics of a monolithic circuit have made possible biasing methods which are far superior to those practically attainable with discrete designs and do not at all suffer from the lack of bypass capacitors.

Probably the most significant application for the circuit in Fig. 2.2 is as the second stage of a differential input, single-ended output amplifier. Examples of this configuration may be seen in the μA702 and the μA710, etc.



(a) Circuit (b) Characteristic

Fig. 2.4 - A Current Source for Generating Very Small Current using Moderate Value Resistors

(B) CONSTANT CURRENT SOURCE

The formation of current sources in the microampere current range can be difficult with integrated circuits because of the relatively large resistance values usually required. A circuit is shown in Fig. 2.4 which makes possible a current source with outputs in tens of microamperes using resistances of only a few kilohms. It makes use of the predictable difference of the emitter-base voltage of two transistors operating at different collector currents. Its operation can be described as follows.

The collector current of a transistor is given as a function of emitter-base voltage by

$$I_C = I_S \exp. \left(q \frac{V_{BE}}{kT}\right) \qquad \ldots\ldots\ldots\ldots\ldots (4)$$

$$\text{for } V_{BE} > \frac{4kT}{q}$$

where K = Boltzmanns Constant

T = Absolute Temperature °Kelvin

q = Electron Charge

This expression holds up to high currents where emitter contact and base spreading resistances become important and down to low currents where collector leakage currents cause inaccuracy.

Solving equation (4) for V_{BE} gives

$$V_{BE} = \frac{kT}{q} \log_e \frac{I_C}{I_S} \qquad \text{..... (5)}$$

This expression can be used to find the emitter-base voltage difference between two transistors:

$$\Delta V_{BE} = V_{BE1} - V_{BE2}$$

$$= \frac{kT}{q} \log_e \frac{I_{C1}}{I_{S1}} - \frac{kT}{q} \log_e \frac{I_{C2}}{I_{S2}}$$

$$= \frac{kT}{q} \log_e \frac{I_{C1}}{I_{C2}} + \frac{kT}{q} \log_e \frac{I_{S2}}{I_{S1}} \qquad \text{..... (6)}$$

For equal collector currents, this becomes

$$\Delta V_{BE} = \frac{kT}{q} \log_e \frac{I_{S2}}{I_{S1}} \qquad \text{..... (7)}$$

Considerable testing has shown that for adjacent, identical integrated circuit transistors this term is typically less than 0.5 mV. It is also relatively independent of the current level, as might be expected since I_S should be a constant. Hence, the emitter-base voltage differential between adjacent integrated circuit transistors operating at different collector currents is given by:

$$\Delta V_{BE} = \frac{kT}{q} \log_e \frac{I_{C1}}{I_{C2}} \qquad \text{..... (8)}$$

within a fraction of a millivolt.

With the circuit in Fig. 2.4 (a) a relatively large collector current is passed through the diode-connected biasing transistor, TR_1. Its emitter-base voltage is used to bias the current source transistor, TR_2. If the base currents of the transistor are neglected for simplicity, the resistance required to determine the current-source current is given by:

$$R_2 = \frac{\Delta V_{BE}}{I_{C2}} = \frac{kT}{qI_{C2}} \log_e \frac{I_{C1}}{I_{C2}} \qquad \text{..... (9)}$$

or for the circuit in Fig. 2.4:

$$R_2 = \frac{kT}{qI_{C2}} \log_e \left(\frac{V^+ - V_{BE1}}{R_1 I_{C2}} \right) \qquad \text{..... (10)}$$

One interesting feature of this circuit is that for $V^+ \gg V_{BE}$ and $I_{C1} \gg I_{C2}$ the output current will vary roughly as the logarithm of the supply voltage (V+). Therefore, if the current source is used in such an application as the input stage of an operational amplifier, the operating collector current and voltage gain of the input stage will vary little over an extremely wide range of supply voltages.

From equation (8) it can be seen that the emitter-base voltage differential is linear function of absolute temperature. Therefore, it might be expected that the output current of the current source would vary in a similar manner. Such is the case as illustrated in Fig. 2.4 (b).

The plot is for $I_{C1} \approx 50\ I_{C2}$ with both zero temperature-coefficient resistors and high resistivity diffused resistors (bulk impurity concentration less than 10^{17} atoms per c.c.). It is notable that diffused resistors provide over-compensation for this characteristic.

(C) LEVEL SHIFTING

Frequently in the design of linear integrated circuits some form of D.C. level shifting is required in the signal path. With discrete designs this can be accomplished by using complementary transistors or, perhaps, Zener diodes. Both these approaches, however, can have their limitations with respect to integrated circuits.

A circuit which avoids many of the previous problems is shown in Fig. 2.5.

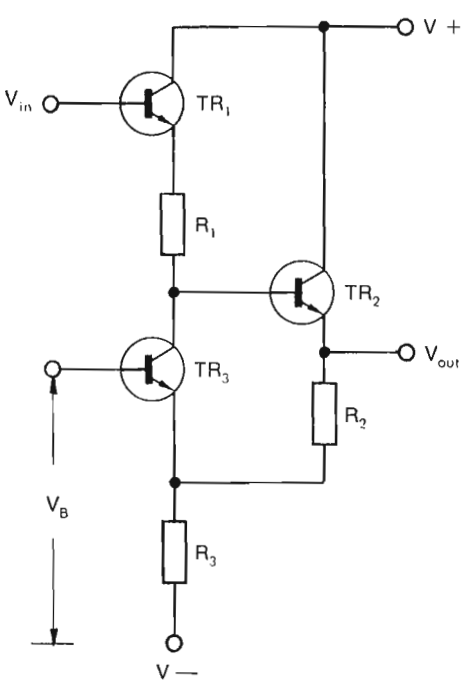


Fig. 2.5 - Circuit for Providing DC Level Shifting as well as Signal Gain

It uses only NPN transistors and its operation can be made essentially dependent only on resistor ratios. TR_1 serves as an input buffer, and the level shifting is accomplished by the voltage-drop across R_1 due to the collector current of TR_3. Feedback from the output, through R_2, is used to increase this voltage drop for negative-going output swings and decrease it for positive-going signals. Properly designed, the stage will give a substantial voltage gain, high input impedance, a low output impedance and a maximum available output swing nearly equal to the supply voltages, in addition to the D.C. level shift.

Assuming that $V^+ + V^- \gg V_{BE}$ and that gain is less than about 5, the voltage gain of the circuit can be obtained from:

$$\Delta V_{out} = \Delta V_{in} - R_1 \Delta I_{C3} \qquad \text{..... (11)}$$

$$\text{where } \Delta I_{C3} = -\frac{\Delta V_{uot}}{R_2} \qquad \text{..... (12)}$$

$$\text{hence, } \Delta V_{out} = \Delta V_{in} + \frac{R_1}{R_2} \Delta V_{out} \qquad \text{..... (13)}$$

$$\text{and } A_V = \frac{\Delta V_{out}}{\Delta V_{in}} = \frac{1}{1 - \frac{R_1}{R_2}} \qquad \text{..... (14)}$$

The output impedance can be approximated by:

$$R_{out} = \frac{R_1 A_V}{h_{FE2}} \qquad \text{..... (15)}$$

The input impedance is usually negative so it is required that the level shifting stage be driven from a low-impedance source for stability. Sufficient conditions for stability are:

$$R_S \ll \frac{h_{FE1} R_2}{A_V} \qquad \text{..... (16)}$$

(D) PNP TRANSISTORS

As has been mentioned previously the use of NPN transistors, only, simplifies manufacture by minimising the number of separate diffusion processes necessary. Where it is highly desirable to have a PNP device available in the circuit which is to perform a specific function, various measures may be taken to provide this without additional diffusion steps.

A « vertical » PNP transistor may be obtained by using the NPN base-diffusion for an emitter and the P-type substrate of the integrated circuit for the collector. This « vertical structure » PNP device has a useful current gain, but having its collector in the substrate restricts its position in the circuit since it will always be electrically connected to the most negative potential.

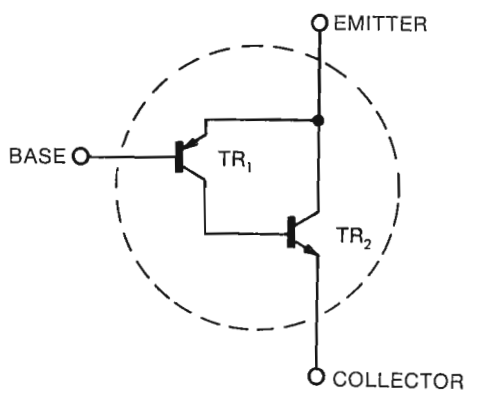
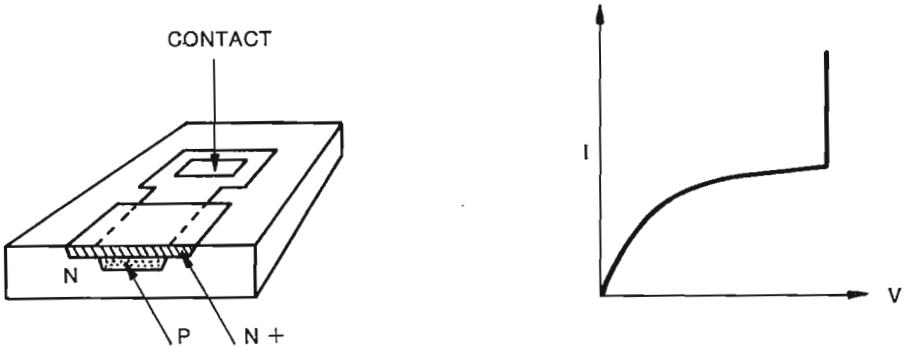


Fig. 2.6 - Composite PNP Transistor



(a) Structure

(b) Characteristics

Fig. 2.7 - Pinch Resistors

Another approach is to form a « surface or lateral » PNP device. It is made using what is usually an NPN base-diffusion for an emitter. This is sorrounded concentrically by a second base-diffusion which serves as a collector. The normal NPN collector region is then the PNP base. This structure suffers from a rather wide base, displaying a low current gain (typically 2). However, it has the distinct advantage that it can be made with the standard NPN process with no additional steps or control. The disadvantage of low current gain can be overcome by amplifying the collector current of the PNP transistor with an NPN device as shown in Fig. 2.6. The combined current gain can be made comparable to that of the NPN transistors in the same substrate.

Thus, the availability of PNP devices with comparable performance allows new freedom in design of circuits for economic manufacture in monolithic integrated form.

(E) PINCH RESISTORS

A potentially-useful element in integrated circuits is the pinch resistor. It is an ordinary diffused (base) resistor, the cross-sectional area of which has been effectively reduced by making an emitter diffusion on top of it (see Fig. 2.7 (a)). The emitter diffusion raises the sheet resistivity from the usual 100 or 200 ohms per square to 10 kilohms per square or higher. This permits rather large resistors to be made in a relatively small area. The pinch resistor, however, has several limiting characteristics. As can be seen from Fig. 2.7 (b) it is linear only for small voltage drops; and it has a low breakdown voltage (5 V to 10 V). Neither the linear nor the non-linear portions of the characteristics can be controlled well and the resistance at the origin can easily vary over a 4:1 range in a normal production run. In addition, the resistor has a very strong positive temperature coefficient, changing by about 3:1 over the — 55°C to + 125°C temperature range.

On the other hand, there is a strong correlation between the pinch resistor values and the transistor current gains obtained in manufacture. The resistors are roughly proportional to the current gains. Furthermore, the resistors tend to track with the current gains over temperature. The matching of identical pinch resistors is also nearly as good as base resistors, and substantially better than transistor current gains.

Fig. 2.3 provides an example of where pinch resistors can be used effectively. Both R_3 and R_4 have small voltage drops across them, and it would be advantageous to have these resistor values proportional to the transistor current gain to obtain the highest possible input impedance consistent with satisfactory bias stability.

Another application is the preamplifier shown in Fig. 2.8 which was designed as part of a hearing aid amplifier. With hearing aids, the maximum supply voltage is usually 1.55 V so the voltage sensitivity and low breakdown of pinch resistors is of little concern. Power drain is, however, a problem, so large resistances are needed. In this circuit, only matching of the pinch resistors (R_1, R_2 and R_3) is required for proper operation. The fact that the pinch resistors correlate with current gain makes the circuit far less sensitive to current gain variations: the pinch resistors and current gains can be varied simultaneously over a greater than 7:1 range without any noticeable degradation of performance.

The above examples show that even though pinch resistors have extremely poor characteristics by discrete component standards, certain characteristics, mainly good matching, a correlation between resistor values and current gain and high sheet resistivities make them extremely useful elements in circuit design. In many cases, the pinch resistors would actually function better than precision resistors if the circuit was designed accordingly.

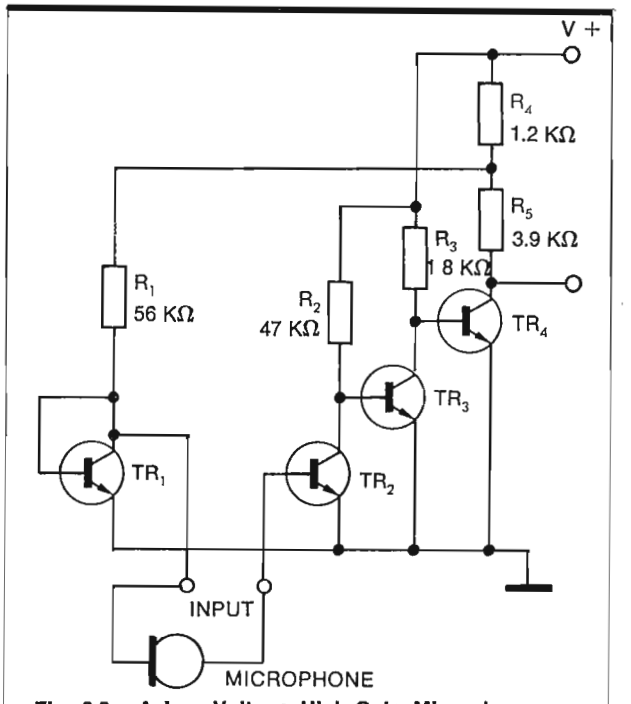


Fig. 2.8 - A Low-Voltage High-Gain Microphone Pre-Amplifier illustrating the use of Pinch Resistors

2.2 DEFINITION OF COMMONLY-USED TERMS

2.2.1 Terms Applicable to Operational Amplifier (e.g. the μA702A and μA709)

INPUT OFFSET VOLTAGE - That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may be also defined for a case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT - The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE - The resistance, looking into either input terminal with the other grounded.

INPUT BIAS CURRENT - The average of the two input currents.

INPUT VOLTAGE RANGE - A range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO - The ratio of the input voltage range to the maximum change in input offset voltage over this range.

LARGE-SIGNAL VOLTAGE GAIN - The ratio of the maximum output voltage swing (with load) to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING - The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE - The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

POWER CONSUMPTION - The D.C. power required to operate the amplifier with the output at zero and with no load current.

SUPPLY VOLTAGE REJECTION RATIO - The ratio of the change in input offset voltage to the change in supply voltage producing it.

TRANSIENT RESPONSE - The closed-loop step function response of the amplifier under small-signal conditions.

PEAK OUTPUT CURRENT - The maximum current that may flow in the output load without causing demage to the unit.

2.2.2 Terms Applicable to Voltage Comparators (e.g. the μA710 and μA711)

LOGIC THRESHOLD VOLTAGE - The approximate voltage at the output of the comparator at wich the loading logic circuitry changes its digital state.

INPUT OFFSET VOLTAGE* - The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT* - The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT* - The average of the two input currents with the output at the logic threshold voltage.

INPUT VOLTAGE RANGE - The range of voltage on the input terminals for which the comparator will operate within specifications.

DIFFERENTIAL INPUT VOLTAGE RANGE* - The range of voltage between the input terminals for which operation within specifiications is assured.

VOLTAGE GAIN* - The ratio of the change in output voltage to change in voltage between input terminals producing it with the D.C. output level in the vicinity of the logic threshold voltage.

RESPONSE TIME* - The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level in excess of that required to just barely bring the output from saturation to the logic threshold voltage. This excess is referred to as the logic overdrive.

OUTPUT RESISTANCE - The resistance looking into the output terminal with the D.C. output level at the logic threshold voltage.

PEAK OUTPUT CURRENT - The maximum current that may flow into the output load without causing damage to the comparator.

POSITIVE OUTPUT LEVEL* - The D.C. output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE OUTPUT LEVEL* - The D.C. output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

POWER CONSUMPTION - The D.C. power into the amplifier with no output load. The D.C. power will vary with signal level, but is specified as a maximum for the entire range of input signal conditions.

OUTPUT SINK CURRENT - The maximum negative current that can be delivered by the comparator.

STROBE RELEASE TIME* - The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from the zero to the one logic level. Appropriate input conditions are assumed.

STROBED OUTPUT LEVEL* - The D.C. output voltage independent of input voltage, with the voltage on the strobe terminal equal to or less than a minimum specified amount.

STROBE CURRENT - The maximum current drawn by the strobe terminal when it is at the zero logic level.

* For the μA711 these definitions apply for either side with the other disabled with the strobe.

2.3 DESCRIPTION OF μA702A CIRCUIT OPERATION

2.3.1 Introduction

The μA702A is a high gain amplifier whose operating characteristics are mainly determined by the use of external feedback elements. It is useful as a general-purpose D.C. or A.C. amplifier to frequencies as high as 30 MHz.

The circuit described below has been designed employing the basic philosophies outlined in Section 2.1. The necessity for high-valued resistors and complementary transistors has been eliminated at no sacrifice to performance. In addition, the important characteristics of the amplifier are dependent only on the matching of components, rather than on their absolute value. The degree of match normally available in integrated circuitry makes any adjustments after manufacture unnecessary.

The active area of the integrated amplifier has been minimised not only to improve high-frequency response, but also to reduce the possibility of crystalline defects and surface phenomena causing failures. This decreases manufacturing costs as well as increasing reliability. The small size of the circuit is illustrated in Fig. 2.9 where it is compared with an early Planar transistor. Typical internal construction is shown in Fig. 2.10.

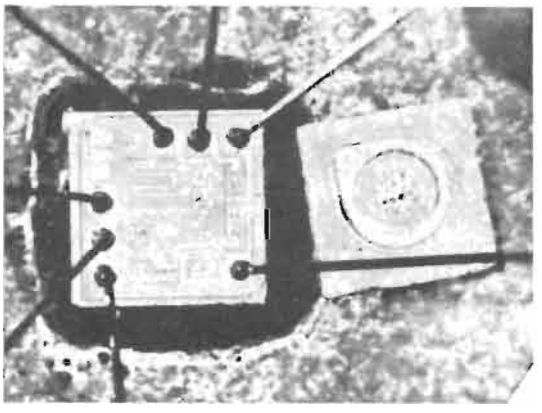


Fig. 2.9 - Comparison of the SGS μA702A (left) with a BFX69 Planar Transistor

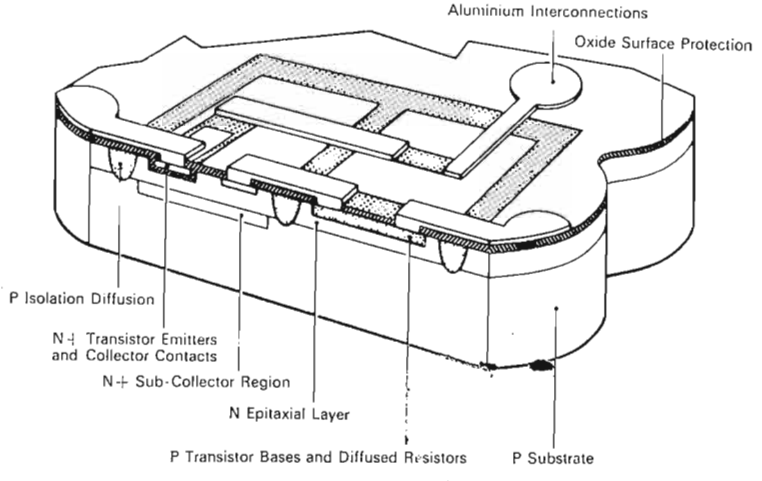


Fig. 2.10 - Sectional View of an SGS Planar Epitaxial Integrated Circuit

2.3.2 Input Stage

In general, the desirable characteristics for an input stage of a D.C. amplifier are low offset voltage, offset current, input current and thermal drift. Matching differential pairs are almost universally used. With this configuration, the input bias of one active device cancels that of the other to give offset and drift dependent only on the degree of match.

In cases where the offset voltage is of prime importance, the bi-polar transistor is undoubtedly the

best choice of an active device for the input stage. Offset voltages of a few millivolts are easily obtained over a wide temperature range. Low input currents and high input impedance can be realised by using very high-gain transistors, and operating them at sufficiently low collector currents.

A Darlington input stage can also be used at some sacrifice in offset voltage, thermal drift and noise figure.

Other active devices, notably the Field Effect transistor, are difficult to match closer than several tens of millivolts. Low offset and drift cannot be obtained without elaborate compensation procedures. Therefore, the use of these devices is limited to cases where offset voltage is of secondary importance and an input current less than a few nanoamps is mandatory. It appears that the most satisfactory compromise for the input stage of a general-purpose amplifier is a matched pair of bi-polar transistors operated at a low collector current. In an integrated circuit, the input stage transistors can be matched quite easily over several decades of collector current by making them with identical structures and locating them phisically close together. There is, however, a problem in obtaining the low collector currents; conventional circuit designs would require large resistance values.

Much reduced resistance values can be used at the expense of input stage gain. Analysis of the problem shows that a low gain in the input stage can be tolerated if the second stage is well balanced. The offset of the second stage appears as an input offset divided by the gain of the input stage.

In the distribution curves obtained in manufacturing an integrated amplifier, the input stage offset will add with the equivalent second stage offset as the square root of the sum of squares. For example, if the gain of the input stage is 2 and the 90% point in the distribution curves for the individual input and second stage offset is 5 mV, the 90% in the distribution of complete amplifiers will be only 5.6 mV. Hence, even with this low gain, the offset contribution from the second stage is quite small.

These facts were used in the design of the input stage. The transistors are operated at 200 μA collector current, but only 2 kΩ collector load resistors are used.

This gives an unloaded differential gain of approximately 15. Therefore, if a balanced second stage design is employed, its contribution to input offset can be made negligible.

The differential input stage (TR_2 and TR_3) and its load resistors (R_1 and R_2) can be seen in Fig. 2.11. The emitters of the input stage are fed from a current source (TR_1) to obtain good input common-mode rejection. The current source is biased from a voltage divider. The V_{BE} of the current source transistor is compensated in the divider with a diode-connected transistor (TR_9).

2.3.3. Second Stage

It is now necessary to design a second stage configuration that will both operate with the small D.C. voltage drops across the input stage load resistors and be inherently as well balanced as the input

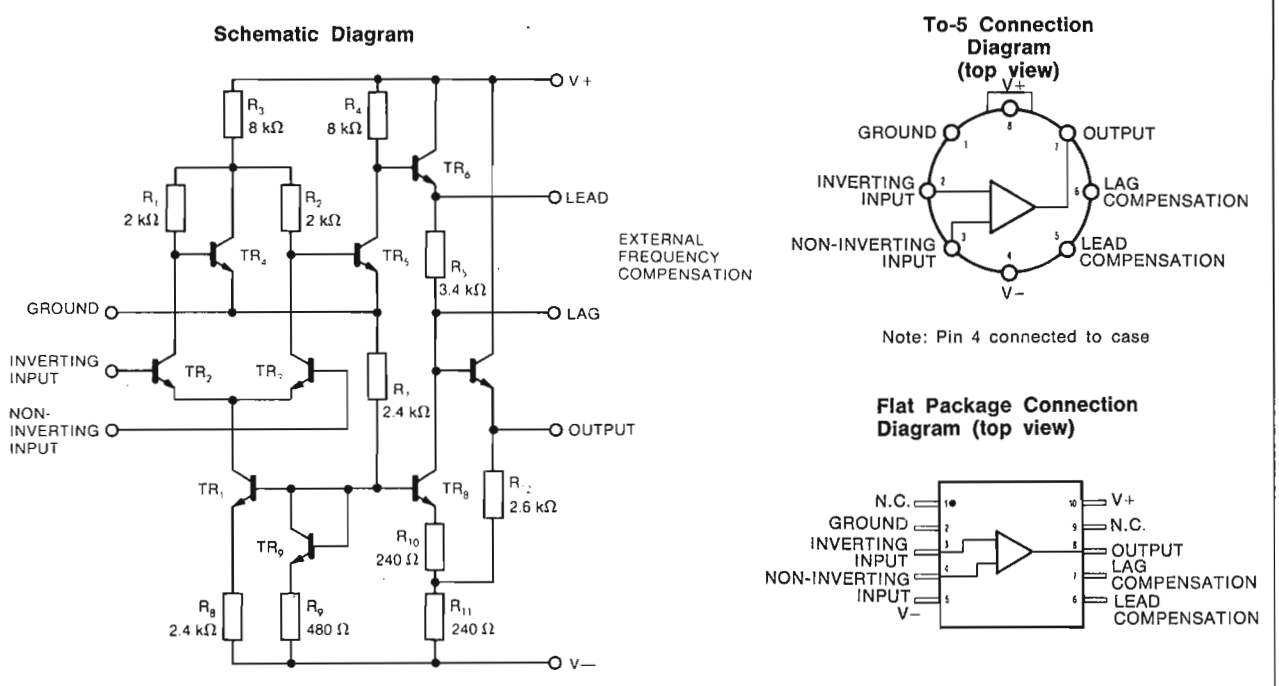


Fig. 2.11 - Circuit Diagram of μA702A

stage. The full differential gain of the input stage should also be used. It would also be of advantage to have a single-ended output since coutinuing with a differential connection to the third stage increases the number of components and creates physical layout problems on the silicon chip.

A connection which satisfies all these requirements is shown in Fig. 2.11.

TR_4 and TR_5 are identical transistors placed close to one another. Their bases are fed from a common voltage point through identical resistors (the input stage load resistors R_1 and R_2). Therefore, when the input stage collector currents are equal, the collector currents of TR_4 and TR_5 will likewise be equal, so that the second stage is balanced. TR_4 also functions as a unity-gain amplifier which inverts the output of TR_2 and combines with the output of TR_3 at the base of TR_5. Therefore, the full differential gain of the input stage is used. A single-ended output is obtained at the collector of TR_5.

An additional feature of this circuit is that, under balanced conditions, the single-ended output of TR_5 is insensitive to changes in positive supply voltage. If the positive supply voltage is increased, the collector currents of both TR_4 and TR_5 will increase such that the voltage on the collector of TR_5 remains constant. If this voltage should change by small amount due to mismatches, the change is divided by a gain of approximately 1000 before appearing as an input-referred error.

Because of the small load resistances of the input stage, the second stage amplifier (TR_5) is essentially voltage driven. Therefore, the gain is not greatly affected by the current gain of TR_5 and is relatively constant over a wide range of operating temperatures.

2.3.4 Output Stage

The first two stages have provided nearly enough voltage gain for the amplifier. Since both positive and negative output swings are desired, some form of D.C. level shifting must be provided as the output of the second stage cannot swing negative. One solution to this problem is to use a PNP transistor both to give level shifting and to provide some additional gain. In monolithic integrated circuits, however this may not always be a convenient answer.

A second approach to level shifting is the use of a Zener diode. One problem here is that Zener diodes are noisy and appreciably affect the overall noise figure of the amplifier. Furthermore. only a single-voltage Zener diode (the emitter-base junction) is usually available in the circuit.

In this amplifier, an entirely new output stage design is used to avoid these difficulties. It incorporates only NPN transistors and no Zener diodes. Its performance is, however, comparable to the best design using complementary transistors.

As can be seen from Fig. 2.11 the output of the second stage is buffered with an emitter-follower, TR_6. A current source (TR_8) provides a voltage drop across R_5 which gives the basic level shifting. An additional emitter-follower (TR_7) is used to give low output impedance. The load resistor of TR_7 is fed back to the emitter of TR_8 giving a controlled amount of positive feed-back. Hence, the output stage actually has a gain in addition to D.C. level shifting. The feedback also enhances the available output swing so that it is nearly equal to the supply voltages.

Summarising the characteristics of this output stage, it has a 200 kΩ input impedance, a 5 V D.C. level shift, a voltage gain of 2.5 and a 200 Ω output impedance. It can deliver a peak-to-peak symmetrical output swing of about 1.8 times the negative supply voltage.

2.3.5 Conditions for D.C. Balance

An interesting feature of the overall amplifier design is that D.C. balance (zero output for zero input) can be obtained independent of the supply voltages and absolute resistors values. This will be shown to hold through to a first approximation in the analysis which follows. Infinite current gains will be assumed for the transistors, as will perfect component matching in some cases. In addition, the emitter-base voltage of certain transistors will be considered equal even though they are operating at different current levels. The latter assumption is not unreasonable in an integrated circuit because the transistor geometries can be scaled in proportion to the operating current.

Using Fig. 2.11 the output voltage can be written as:

$$V_{out} = V^+ - R_4 i_{C5} - R_5 i_{C8} - 2V_{BE} \qquad \text{..... (1)}$$

If the input stage collector currents are equal TR_4 and TR_5 are well matched and R_1 is equal to R_2, then i_{C4} and i_{C5} will be equal. Thus,

$$V^+ - R_3 i_{C5} - \left(R_3 + \frac{R_1}{2} \right) i_{C1} - V_{BE} = 0 \qquad \text{..... (2)}$$

The collector current of TR_8 is given by

$$i_{C8} = - \frac{\dfrac{R_9(V^- + V_{BE})}{R_7 + R_9} - \dfrac{R_{11}(V^- - V_{out})}{R_{11} + R_{12}}}{R_{10} + \dfrac{R_{11}R_{12}}{R_{11} + R_{12}}} \qquad \text{..... (3)}$$

While the collector current of TR_1 is

$$i_{C1} = - \frac{R_9(V^- + V_{BE})}{R_8(R_7 + R_9)} \qquad \text{..... (4)}$$

substituting (3) into (1) yelds

$$\left(1 - \frac{R_5 R_{11}}{R_{10}R_{11} + R_{10}R_{12} + R_{11}R_{12}} \right) V_{out} =$$

$$= V^{\cdot} - R_4 i_{C5} + \frac{R_5\left(\frac{R_9}{R_7+R_9} - \frac{R_{11}}{R_{11}+R_{12}}\right)}{R_{10}+\frac{R_{11}R_{12}}{R_{11}+R_{12}}} V^- +$$

$$+ \left[\frac{\frac{R_9R_5}{R_7+R_9}}{R_{10}+\frac{R_{11}R_{12}}{R_{11}+R_{12}}} - 2\right] V_{BE} \quad \ldots\ldots\ldots (5)$$

Combining (4) and (2) gives

$$V^+ - R_3 i_{C5} + \frac{R_9\left(R_3+\frac{R_1}{2}\right)}{R_8(R_7+R_9)} V^- +$$

$$+ \left[\frac{\left(R_3+\frac{R_1}{2}\right)R_9}{R_8(R_7+R_9)} - 1\right] V_{BE} = 0 \quad \ldots\ldots\ldots (6)$$

For balanced input and second stages, as assumed, the output voltage will be given as a function of circuit parameters by the set of equations (5) and (6). It is desired that the output voltage under these conditions be zero, independet of supply voltages. This can be accomplished by setting the coefficients of V^+, i_{C5} and V^- in (5) equal to the corresponding coefficients in (6). Hence, if

$$R_3 = R_4 \quad \ldots\ldots\ldots\ldots (7)$$

and

$$\frac{R_5\left(\frac{R_9}{R_7+R_9} - \frac{R_{11}}{R_{11}+R_{12}}\right)}{R_{10}+\frac{R_{11}R_{12}}{R_{11}+R_{12}}} = \frac{R_9\left(R_3+\frac{R_1}{2}\right)}{R_8(R_7+R_9)} \quad \ldots\ldots\ldots\ldots (8)$$

Equations (5) and (6) can be combined to give:

$$\left(1 - \frac{R_5R_{11}}{R_{10}R_{11}+R_{10}R_{12}+R_{11}R_{12}}\right) V_{out} =$$

$$= \left[-1 + \frac{\frac{R_9R_5}{R_7+R_9}}{R_{10}+\frac{R_{11}R_{12}}{R_{11}+R_{12}}} - \frac{R_9\left(R_3+\frac{R_1}{2}\right)}{R_8(R_7+R_9)}\right] V_{BE} \quad \ldots\ldots\ldots\ldots (9)$$

substituting (8) Eq. (9) yields

$$V_{out} = - V_{BE} \quad \ldots\ldots\ldots\ldots (10)$$

Since V_{BE} is approximately 700 mV and the open-loop gain of the amplifier is approximately 3000, the input referred offset is roughly 0.23 mV. This is about an order of magnitude smaller than offset due to random mismatching so the output voltage at null given by equation (10) is essentially zero and independent of both the supply voltages.

Furthermore, if every resistor in the circuit is multiplied by any constant, equations (7) and (8) will not be altered. Therefore, the conditions that establish equation (10) are dependent only on resistor ratios — not absolute values.

Rough order of magnitude calculations show that for $h_{FE}>30$ the assumption that h_{FE} is infinite is reasonable. This has been substantiated by experimental work. The effect of current gain on offset was found to be substantially less than the offset due to other causes. In fact, the offsets produced by the differential base currents tend to cancel nearly as well as the current-gain matching of various units will permit.

2.3.6 D.C. Offset and Component Matching

It was assumed previously that certain components were perfectly matched and that the ratio of all resistors was constant. In practice, this is obviously not quite true. The effect of mismatches on offset voltage is briefly examined below.

The sensitivity of the offset voltage to deviations in resistor ratios is conveniently determined by changing, independently, the value of each resistor in the circuit and measuring the effect on offset. This has been done with the amplifier, and the results are given in Table 1.

Resistor	Nominal Value (kΩ)	Change in Offset Voltage (mV)
R_1	2	+ 2
R_2	2	— 2.9
R_3	8	— 0.7
R_4	8	+ 0.5
R_5	3.4	+ 0.3
R_7	2.4	— 0.1
R_8	2.4	+ 0.4
R_9	0.48	+ 0.1
R_{10}	0.24	— 0.1
R_{11}	0.24	— 0.3
R_{12}	2.6	+ 0.2

Table 1 - Change in Input-referred Offset Voltage for 10% Change in Individual Resistor Values

Except for R_1 and R_2, a 10% change in any resistor value has little effect on offset. Since, as has already been mentioned, the actual resistance ratios in integrated circuitry can be held substantially closer than 10%, deviations in the resistance ratios of R_3, R_4, etc. to R_{12}, can be neglected.

Of greatest importance is the matching of R_1 and R_2, rather than the other resistors, because the offsets tend to cancel if both change together, as can be seen from Table 1. For this reason, the techniques outlined in paragraph 2.1 are employed; i.e., they have identical geometric structures, are located close together and have a wider track than the other resistors.

The offset sensitivity to mismatches in transistor parameters can likewise be determined. Experimentation, similar to that used to determine sensitivity to resistor values, has shown that the matching of TR_2 with TR_3 and TR_4 with TR_5 in both current gain and emitter base voltage clearly dominates in determining offset. Every effort was made in mask design to ensure that these pairs would be well matched. First, the devices were located as close together as possible. The small size permitted centre-to-centre spacing of 5 mils. (0.127 mm.). Second, the distance between these transistors and elements dissipating appreciable power was made as large as possible to minimise the effect of thermal gradients.

2.4 SUMMARY OF μA702A PERFORMANCE

2.4.1 Amplifier Basic Characteristics

Typical performance of the amplifier is summarised in Table 2. In general, the μA702C may be used in the circuits described in the Handbook unless specifically stated otherwise. Due regard must be taken, however, of certain relaxations in specifications when calculating drift, etc. Reduction in guaranteed open-loop gain may reduce the stability of the closed-loop gain under varying operating conditions. Details such as maximum operating conditions and tolerance spreads can be obtained from the appropriate data sheets. Inherent balance of the design is demonstrated by the low offset voltage and thermal drift characteristics and excellent supply voltage rejection.

All data for 25°C ambient temperature unless otherwise indicated

	$V^+ = 12$ V $V^- = -6$ V	$V^+ = 6$ V $V^- = -3$ V
Input Offset Voltage	0.5 mV	0.7 mV
Input Offset Current	0.18 μA	0.12 μA
Input Bias Current	2 μA	1.2 μA
Input Resistance	40 kΩ	67 kΩ
Temperature Coefficient of Input Offset Voltage		
$-55°C \leq T_A \leq 125°C$ $R_S = 50\ \Omega$	2.5 μV/°C	3.5μV/°C
Common-mode Rejection Ratio	95 dB	95 dB
Large-Signal Voltage Gain	3600	900
Output Resistance	200 Ω	300 Ω
Output Voltage Swing	± 5.3 V	± 2.7 V
Power Consumption	80 mW	17 mW
Supply Voltage Rejection Ratio	75 μV/V	75 μV/V

Table 2 - Typical Performance of the μA702A Integrated Operational Amplifier

The amplifier may be operated with practically any combination of supply voltages, within certain limits, without greatly affecting offset. The gain and output swing will, of course, be determined by the supply voltages. The indicated 2:1 ratio of positive and negative supply voltages need not be maintained. Increased output swing (up to about ± 7 V) can be obtained with larger negative supply voltages. Little is gained, however, by increasing the negative supply voltages beyond 70% of the positive supply voltages.

The voltage gain and input bias current of the amplifier are roughly proportional to the negative supply voltage.

Fig. 2.12 gives a plot of the open loop gain as a function of temperature.

In general, the amplifier favours high temperature operation for the input resistance and bias current. Since the current gain of the transistors increases at high temperatures, higher input resistance and lower input bias currents are obtained, as shown in Fig. 2.13 and Fig. 2.14. The increased current gain also gives some improvement in balance, gain stability and thermal drift. These facts, along with the small size of the amplifier, indicate that it is well suited to applications where a temperature-stabilizing oven can be used to obtain very low drift. Excellent performance can be obtained even if the temperature control is rather loose.

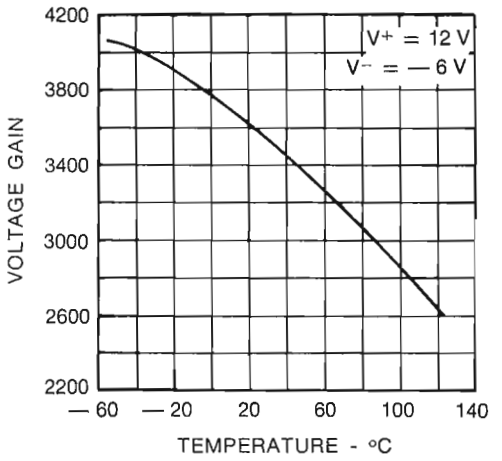


Fig. 2.12 - Voltage Gain as a Function of Ambient Temperature

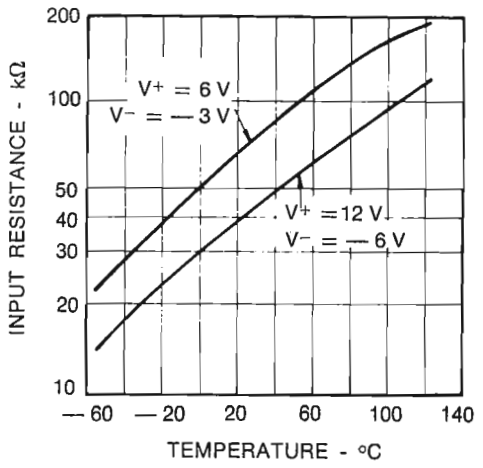


Fig. 2.13 - Input Resistance as a Function of Ambient Temperature

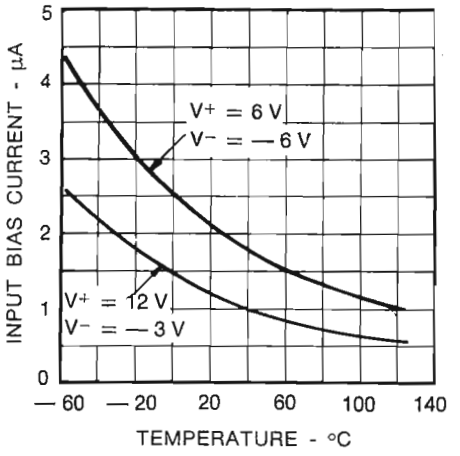


Fig. 2.14 - Input Bias Current as a Function of Ambient Temperature

Some improvement can, in fact, be obtained simply by locating the amplifier at some « hot spot » within the equipment.

The voltage transfer characteristic of the amplifier given in Fig. 2.15 illustrates the output swing capabilities and the linearity. The maximum available symmetrical output swing is plotted as a function of load resistance in Fig. 2.16.

The primary limitation on negative output swing under load is the current available from the output circuit resistor (R_{12}) (see Section 2.3.2, Fig. 2.11) to drive the load with negative outputs. Therefore, the swing can be improved by connecting an external resistor (R_1) between the output terminal and the negative supply voltage as shown in Fig. 2.16. Even larger swings can be obtained if the resistor is returned to a more negative supply. Since the output impedance is quite low, considerable excess current can be drawn in this fashion without affecting offset or gain. Peak currents as high as 50 mA may be obtained from this amplifier.

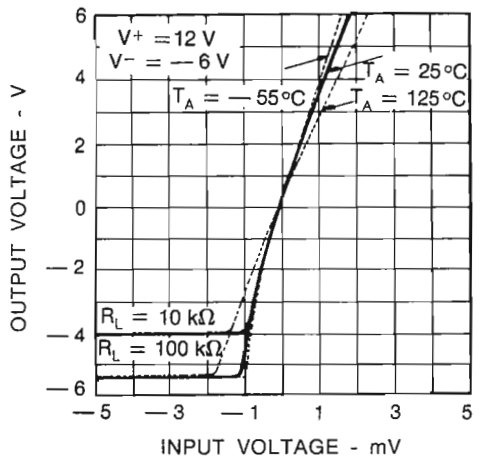


Fig. 2.15 - Voltage Transfer Characteristic

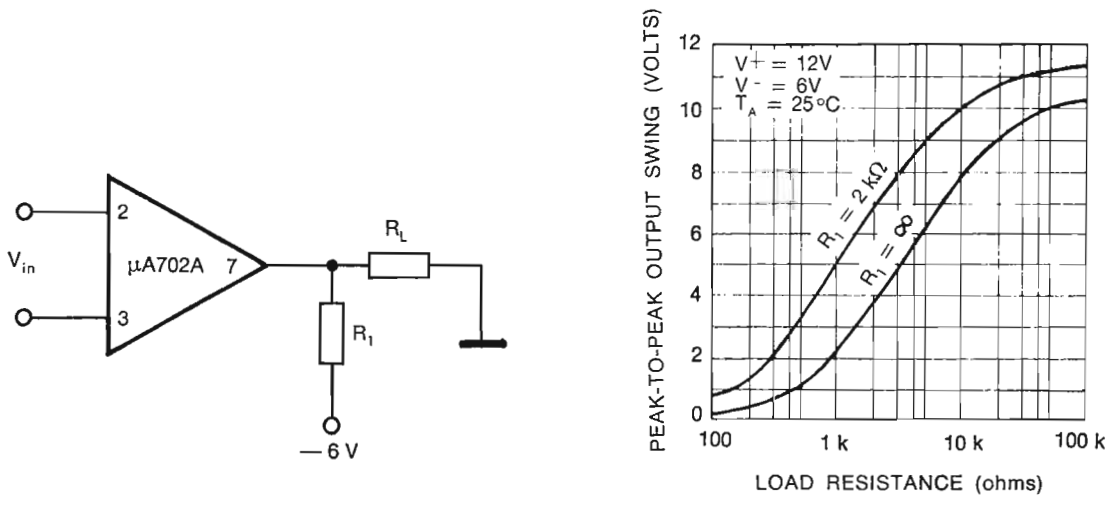


Fig. 2.16 - Maximum Output Swing as a Function of Load Resistance

Since the injection efficiency of TR_7 falls off with increased collector current, for open-loop linear operation it is necessary to limit the output current to 10 mA or less, according to the circuit configuration.

As has been previously mentioned, there is a limit to the maximum negative excursion of the output voltage dependent upon the output load impedance.

The open-loop frequency response of this amplifier is of great importance, as it is primarily designed to be used as a feedback amplifier. Specifically, it is desired that the high-frequency roll-off be less than 12 dB per octave at frequencies where the loop-gain is greater than unity. If this condition is not satisfied, the amplifier will oscillate when feedback is applied.

The open-loop frequency response of the amplifier is plotted in Fig. 2.17.

The high-frequency roll-off approches 12 dB per octave at 7 MHz for an open-loop gain of somewhat less than 50 dB. Therefore, the amplifier is stable for closed-loop gains higher than 50 dB. To illustrate the point, a typical circuit for a 46 dB amplifier is shown in Fig. 2.18 along with the closed-loop frequency response.

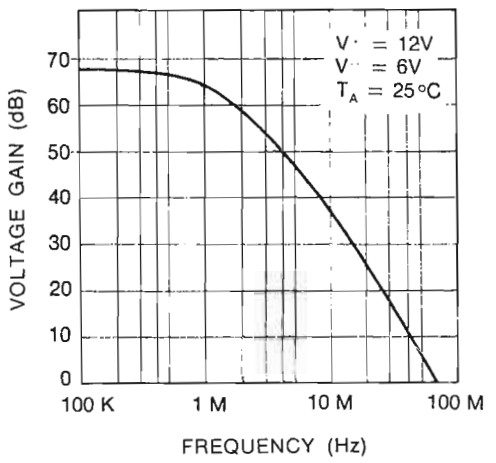
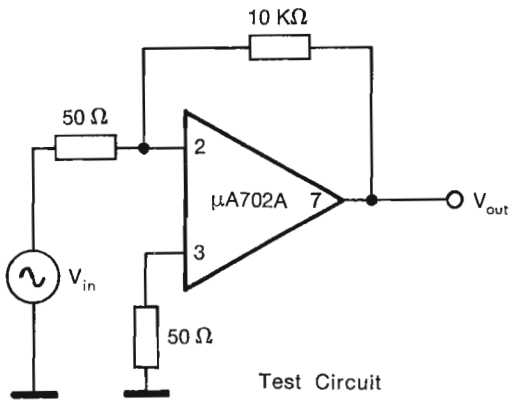


Fig. 2.17 - Open-loop Frequency Response



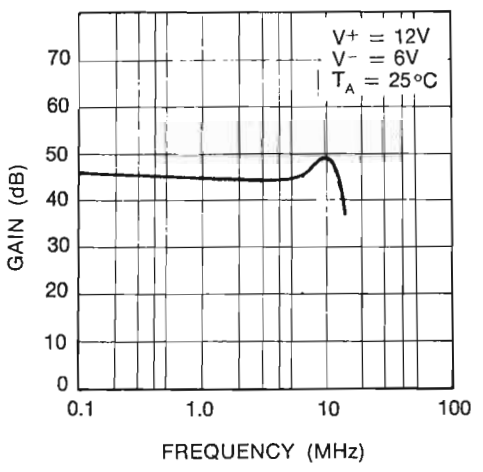


Fig. 2.18 - Closed-loop Frequency Response of a « X200 » Amplifier without External Frequency Compensation

It can be seen that there is almost 6 dB of peaking at the high-frequency end, indicating that the phase margin is probably less than 30°. For most practical circuits, in order to ensure stability under adverse conditions, it is usual to specify a minimum phase margin of 45°.

This would correspond to a maximum peaking at the high-frequency end of approximately 3 dB.

As shown in Fig. 2.18 the bandwidth of the amplifier is extended by application of feedback. However, the full output swing of the amplifier cannot be obtained over this extended frequency range. The basic frequency limitations of the output swing are indicated in Fig. 2.19. The subject of frequency compensation and stability is more fully discussed in Section 5.

Due mainly to internal capacitance effects, the very high common-mode rejection ratio of this amplifier is reduced at high frequencies. Since the capacitance of the input stage has more effect with high source impedance, the common-mode rejection ratio is also a function of this circuit condition. Fig. 2.20 illustrates this relationship.

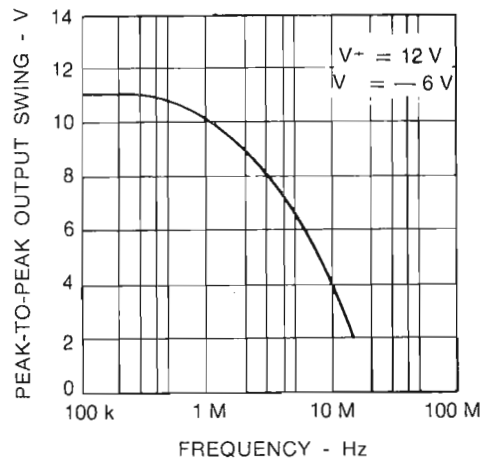
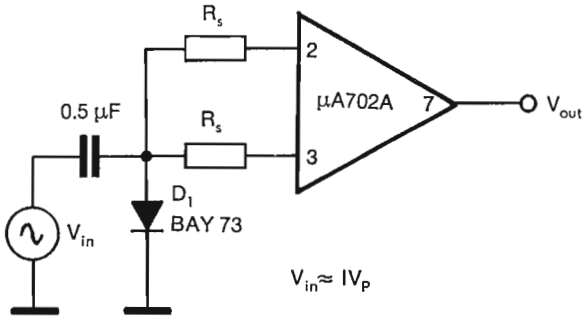


Fig. 2.19 - Maximum Output Swing as a Function of Frequency



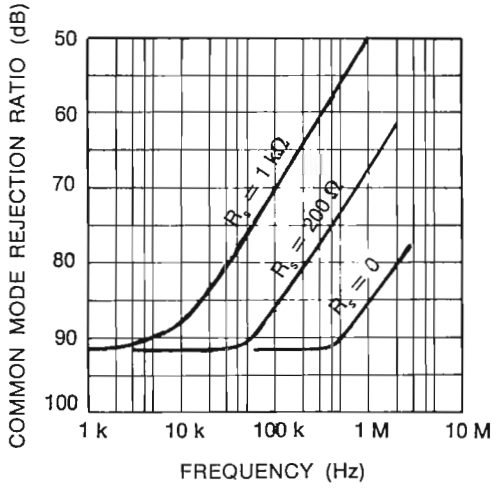


Fig. 2.20 - Common Mode Rejection Ratio as a Function of Frequency for Various Source Resistances (µA702A)

2.4.2 Prevention of Input Latch-up Conditions

From the circuit diagram of the amplifier, reference Section 2.3, Fig. 2.11, it can be seen that, if the input voltage on the inverting input terminal exceeds $2\,V_{BE}$, the input stage transistor will saturate.

If this happens, the circuit will still have gain but the inverting input will now act as a non-inverting input. Therefore, it is important to ensure that large output swings cannot saturate the input stage through the feedback network, as this can result in positive feedback and a latch-up condition. If the feed-back path from the output has a sufficiently low impedance, the resulting current flowing at the collector-base junction of TR_2 and the emitter-base junction of TR_4 can reach levels at which permanent damage may occur.

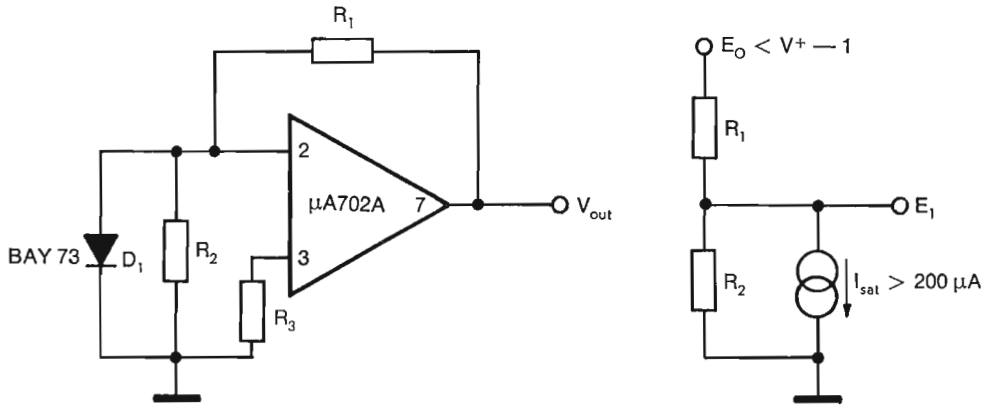
To saturate the input stage, the maximum common-mode voltage on the input terminal must be exceeded, and enough current must be supplied to saturate the input stage (a current nearly equal to the collector current of TR_1 would be required). In general, this is not a problem if the closed-loop gain is greater than 10 or if the feedback resistor between the output and inverting input terminals is greater than 50 kΩ. If there is any doubt, the latch-up condition can be positively eliminated by connecting a limiting diode between the inverting input terminal and ground as shown in Fig. 2.21 (a).

If it is desired to determine whether a certain feedback configuration can produce latch-up, the equivalent circuit in Fig. 2.21 (b) can be used. The maximum output voltage of the amplifier is about 1 V

less than the positive supply voltage (V^+), the minimum current that will saturate the input stage is 200 μA and the minimum input voltage for saturation is 0.5 V.

Therefore, sufficient conditions for the elimination of latch-up are:

$$E_1 < 0.5\,V < R_2 \frac{(V^+ - 1)}{R_1 + R_2} - R_1 I_{sat} \qquad \ldots\ldots\ldots\ldots (1)$$



(a)
Feedback Circuit and Limiting Diode

(b)
Equivalent Circuit for Latching Condition

Fig. 2.21 - Circuits Used to Determine whether Limiting Diode is needed to Prevent Possible Latch-up Condition

Two other circuits which are potentially prone to latch-up conditions are shown in Fig. 2.22 and 2.23. Transients present at the output can drive the amplifier beyond its positive common-mode limit through the integrating capacitor C_1.

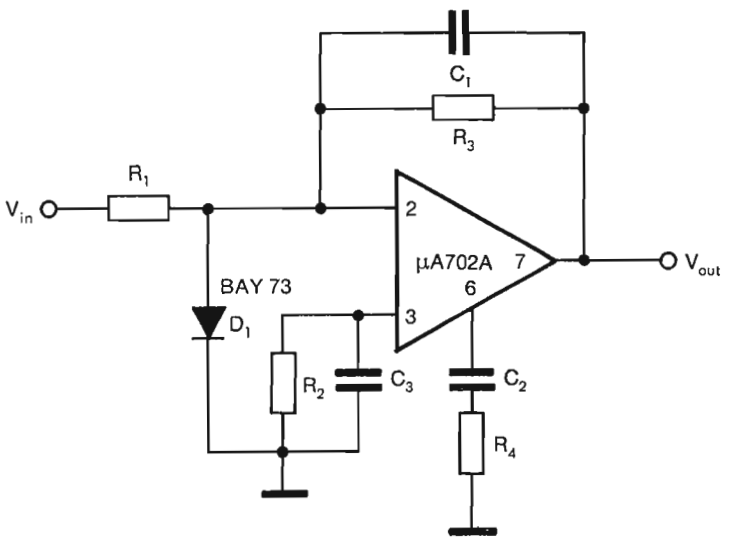


Fig. 2.22 - Integrator Circuit with Latch-up Protection

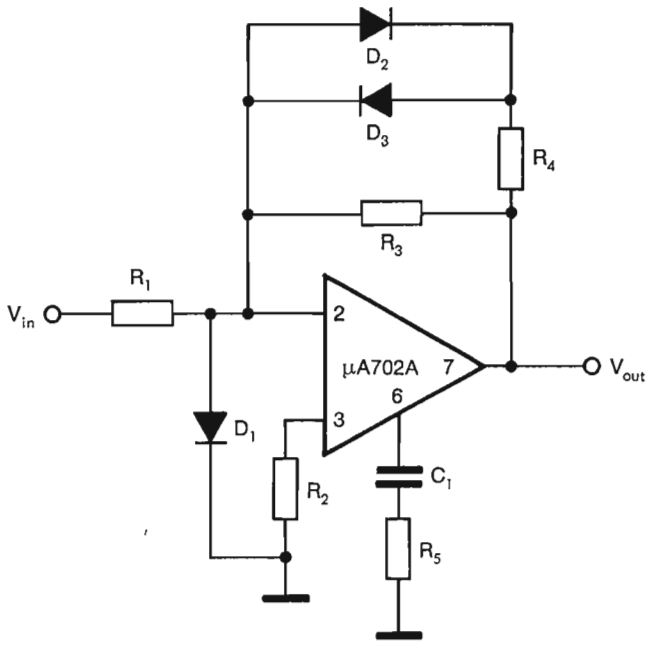


Fig. 2.23 - Non-linear Amplifier with Latch-up Protection

This current can reach destructive levels if the integrating capacitor is more than 10 times larger than the frequency compensating capacitor on pin (6). The clamping diode, however, completely eliminates the problem. A sufficiently large compensating capacitor will limit the peak diode current to a reasonable value.

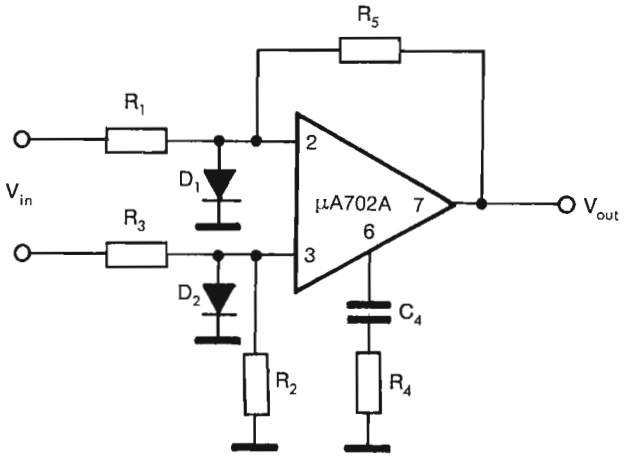
The amplifier circuit shown in Fig. 2.23, which has a nonlinear (clipping) transfer characteristic, is also vulnerable to a latch-up condition, due to the possibility of excessive current flowing throug D_3 to the inverting input terminal pin (2). Here again, the inclusion of D_1 eliminates the problem. R_4 has been included to limit the maximum possible current flowing through D_3 and D_1.

2.4.3 General Circuit Precautions

The previous section describes how the possibility of input latch-up and consequent circuit malfunction may be guarded against by the use of diodes at the input terminal.

A diode used in a similar configuration is a useful means of protecting input where there is risk of large input transients occurring.

Fig. 2.24 shows an example where the μA702A, used as a differential amplifier, is protected against positive transients at both inputs. Additional diodes connected with reversed polarity would provide negative transient protection, although, as can be seen from the specifications, these would not normally cause damage unless they exceeded —5 V in magnitude.



$D_1 = D_2 =$ BAY 73

Fig. 2.24 - Input Transient Protection

In order to ensure that no damage to the output stage can occur, certain precautions should be observed.

As indicated by the data sheets, peak output current should not exceed 50 mA. This does not necessarily allow the output to be short-circuited with safety, even for short periods, since the current may well exceed this value with consequent overheating of the output transistor.

Average output current is determined by total internal power dissipation considerations. 200 mW for the flat package and 300 mW for the the TO 5 can will allow operation in ambient temperatures up to 100°C.

Using positive 12 V and negative 6 V power supplies, this would give 3 mA and 8 mA as a conservative estimate for the maximum average current for the flat package and TO 5 can respectively.

Considerably greater average current may safely be obtained where reduced maximum ambient temperature can be guaranteed, lower power supplies and efficient heat-sinks are available. In case of uncertainty the manufacturers should be consulted.

Fig. 2.25 shows a circuit configuration which could result in excessive current from the amplifier. Unless a resistor (R_2) is inserted in series with the base of the following transistor, it is possible for that stage to saturate and current to flow via the comparatively-low-valued emitter resistor R_1 to earth.

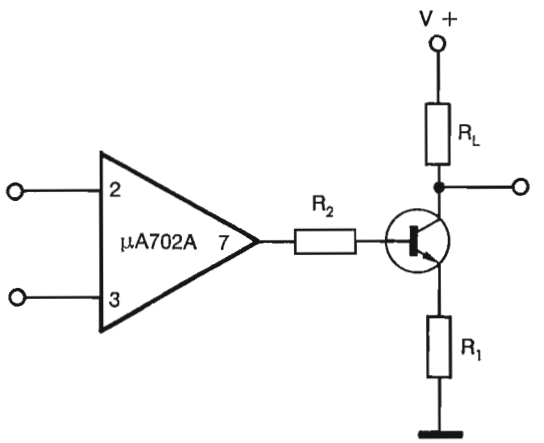


Fig. 2.25 - Output Current Limiting

There is a possibility that excessive peak current may be delivered by the amplifier under certain conditions if the load is highly capacitive. In this case the circuits shown in Fig. 2.26 may be used for protection. In Fig. 2.26 (a) a resistor (R_5) in series with the output is used to limit the peak current charging C_L. Bearing in mind that the typical open-loop internal impedance of the amplifier is 200 ohms, an

additional resistor of 270 ohms would provide adequate protection for worst-case conditions. Another approach is shown in Fig. 2.26 (b), a capacitor is connected between the lag compensation point (pin 6) and earth which has a value equal to, or greater than, one-tenth the value of the effective parallel-load capacitance. By this means the « slewing » rate is limited to a value which prevents excessive output current. It should be noted that both the circuits will restrict the bandwidth of the amplifier.

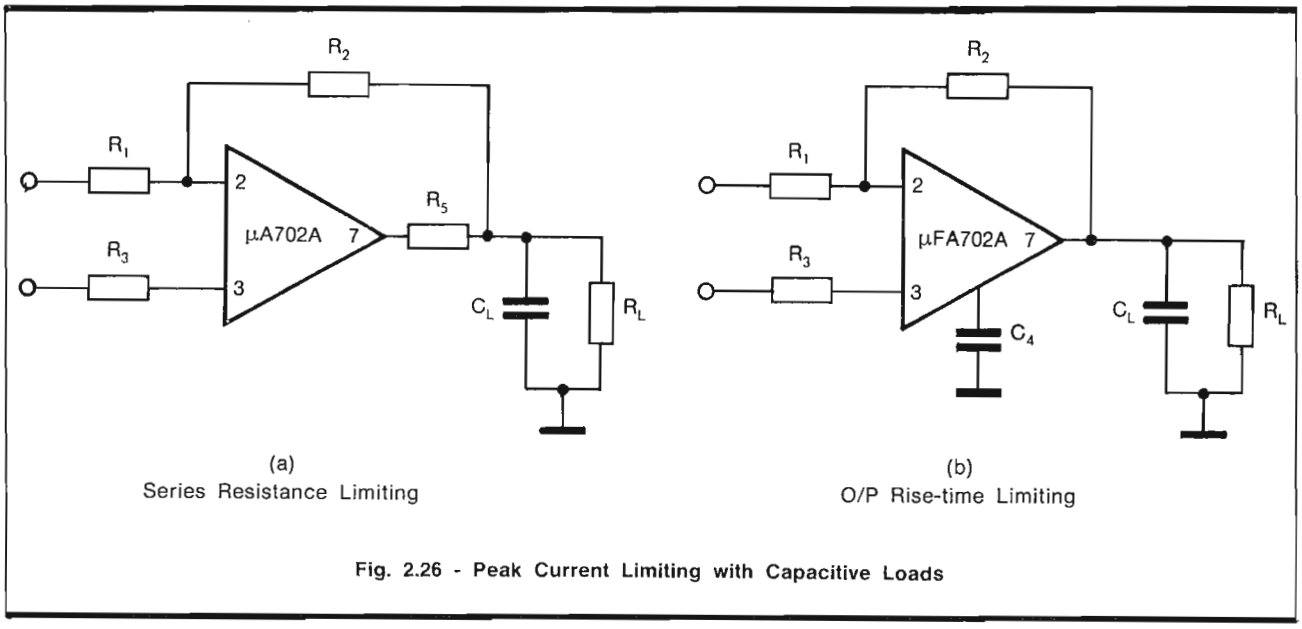


Fig. 2.26 - Peak Current Limiting with Capacitive Loads

If the μA702A is used to drive logic circuits it is important to limit the maximum output swing of the amplifier, both because damage might be caused to the input of the logic integrated circuits and because excessive current might flow through the output transistor as a result, for example, of forward biasing any of the isolation PN junctions within the logic element.

Fig. 2.27 shows a method which effectively overcomes the above problems. The D_1 prevents negative excursions of the amplifier from exceeding approximately —0.7 V (the internal impedance of the amplifier for negative swings limits the output current to a safe value).

The diode D_2 connected between pin (6) (i.e. the lag frequency compensation point which is equivalent to the base of the output emitter-follower) and the positive rail of the logic supply will prevent the output voltage from rising above that of the logic supply.

If the μA702A is used to drive an RT L micrologic family, it is also necessary to insert a 640 ohms resistor in series with the output. In these conditions, the fan-out of the μA702A is 5. A fan-out of up-to 10 can be obtained by reducing the resistor at the output to 320 ohms.

For the DT L micrologic family, the fan-out is limited to 1. A higher fan-out is available if a resistor is connected between the amplifier output and the power supply negative terminal. A 3.9 kΩ resistor will allow a fan-out of 2 and that of 2 kΩ provides a fan-out of 3.

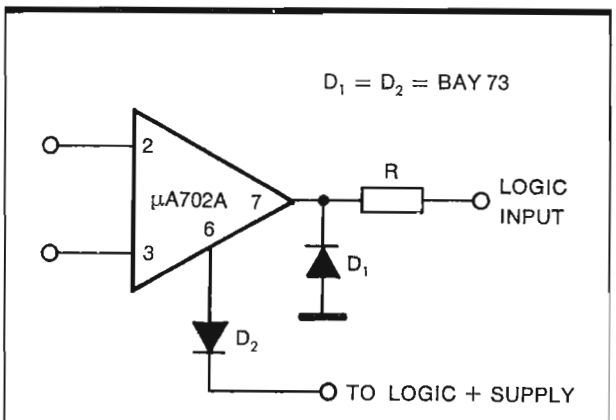


Fig. 2.27 - Logic Compatibility

2.5 DESCRIPTION OF μA709 CIRCUIT OPERATION

2.5.1 Introduction

The μA709 is a high-gain operational amplifier intended for use in D.C. servo systems and high impedance analogue computers, also for low-level instrumentation applications and for the generation of special linear and non-linear functions.

The circuit described below has been designed employing the basic philosophies outlined in Section 2.1. It gives a performance which is comparable to the best discrete component designs, yet it is relatively simple to build in monolithic form. It features low offset, high input impedance, a large input common mode range, high gain, low power consumption and a large output swing under load. The amplifier displays exceptional temperature stability and will operate over a wide range of supply voltages with little degradation of performance. The suitability of the circuit for integration is indicated by the fact that it is constructed on a 0.035 mm^2 silicon die using a six-mask Planar epitaxial process which is nearly indentical to that employed with common digital integrated circuits. A photomicrograph of an actual amplifier is shown in Fig. 2.28.

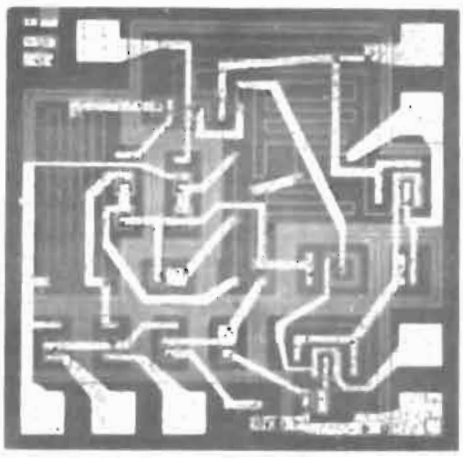


Fig. 2.28 - Photomicrograph of the SGS μA709 High Performance Operational Amplifier

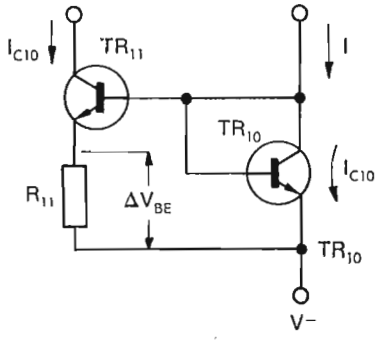
2.5.2 Input Stage

Darlington-input amplifiers have generally been used in microcircuits requiring high input impedance because of restrictions on maximum resistance values, which make it difficult to operate transistors at low collector currents. With D.C. amplifiers, the Darlington connection has the disadvantage of considerably higher offset and thermal sensitivity than a non-Darlington differential pair. In addition, input impedance and input currents vary as the square of the current gain with a Darlington connection, so it does not provide a great performance advantage when full temperature range operation is considered.

The described design is a departure from this conventional approach: the input stage is operated at low collector currents but without requiring usually large resistance values.

One unusual feature of the input stage is the current source for the emitters of the input transistors which is shown in Fig. 2.29.

It makes use of the highly predictable difference in the emitter-base voltage of two identical transistors operating at different collector currents to form a microampere current source using resistances of only a few kilohms.



$$\Delta V_{BE} = V_{BE10} - V_{BE11}$$

$$= \frac{KT}{q} \log_e \frac{I_{C10}}{I_{C11}}$$

$$I_{C11} \cong \frac{\Delta V_{BE}}{R_{11}}$$

Fig. 2.29 - Simplified Circuit of Input Stage Current Source

With reference to Fig. 2.29, a relatively-large current (I) is passed through the diode-connected transistor, TR_{10}. Assuming large current gains for TR_{10} and TR_{11}, the collector current of TR_{10} will be equal to this current. The emitter-base voltage of TR_{10} is used to bias the current source, TR_{11}. The resistor in the emitter of TR_{11} determines the collector current of the device.

This type of current source is described in detail in Section 2.1.2; but to give an example of its operation, it might be assumed that the biasing transistor TR_{10} is operating at 1 mA collector current and that it is desired to operate TR_{11} at 10 μA. For this ratio of collector currents, the emitter-base voltage difference between the two devices will be 120 mV at room temperature (60 mV/decade). Therefore, it is only necessary to insert a 12 kΩ resistor in the emitter of TR_{11} to obtain the desired 10 μA collector current.

The differential input stage (TR_1 and TR_2) and its collector load resistors (R_1 and R_2) are shown in the complete circuit of Fig. 2.32. The input stage operates at approximately 20 μA collector current. The collector load resistors are relatively small for this current level, but they do provide enough gain to make the effect of second stage offset small if the second stage is reasonably well balanced.

Another interesting feature of this input stage is that the variation in current-source current with temperature almost exactly compensates for the variation in input stage transconductance. As a result, the voltage gain holds constant, within a few percent, over the full operating temperature range of the circuit. In addition, the collector current of the current source is roughly proportional to the logarithm of the collector current of its biasing transistor. Since the collector current of the biasing transistor varies approximately as the supply voltage, the input stage operating level is practically unaffected by supply voltage changes.

2.5.3 Second Stage

The second stage design is similar to that described in Section 2.1.2. A simplified circuit is shown in Fig. 2.30.

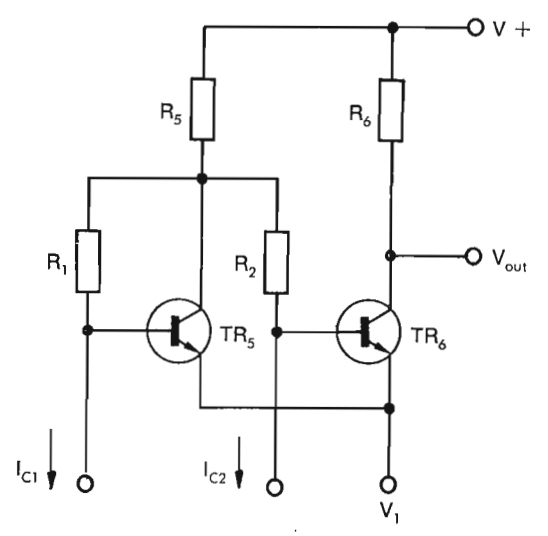
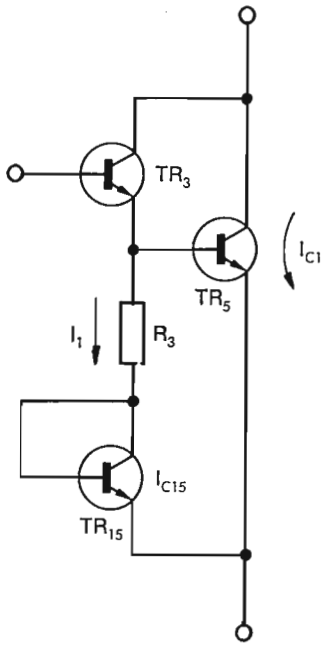


Fig. 2.30 - Simplified Circuit of Second Stage



$$\Delta V_{BE} = V_{BE5} - V_{BE15}$$

$$= \frac{KT}{q} \log_e \frac{I_{C5}}{I_{C15}}$$

$$I_1 = \frac{\Delta V_{BE}}{R_1}$$

Fig. 2.31 - Circuit Illustrating Principle of the Modified Darlington Connection

The input stage collectors are connected to the bases of the second stage transistors. The collector load resistors of the input stage, R_1 and R_2, are connected as shown. In the simplified circuit, TR_6 is the second stage amplifier while TR_5 provides balanced biasing. TR_5 also serves as a unity gain inverter, delivering the full differential output of the input stage to the base of TR_6. This helps to minimise offset and thermal drift since the input stage has low gain because of the low-value collector load resistors. As pointed out in Section 2.1.2, this second stage design is extremely useful in going from a differential to a single-ended connection in that it provides excellent isolation to variations in supply voltage when R_5 and R_6 are equal.

The actual circuit employed is shown in Fig. 2.32. A modified Darlington connection is used in the second stage to prevent loading of the input stage. This makes the second stage gain proportional to the predictable transconductance characteristic of the transistors, rather than the current gain.

A unique scheme is used to make the Darlington-connected second stage insensitive to high temperature leakages and stabilize it over the operating temperature range. This is shown in Fig. 2.31. The conventional way of accomplishing the task would be to connect a resistor across the emitter-base junction of TR_5. However, the required value of resistance would be large; and since the emitter-base voltage has a negative, and the resistor a positive temperature coefficient, the bleed current would become small at high temperatures where it is needed most and large at low temperatures where it is undesirable. However, with the scheme in Fig. 2.31, resistance values more than an order of magnitude lower can be used, and the bleed current has a strong positive temperature coefficient, as desired.

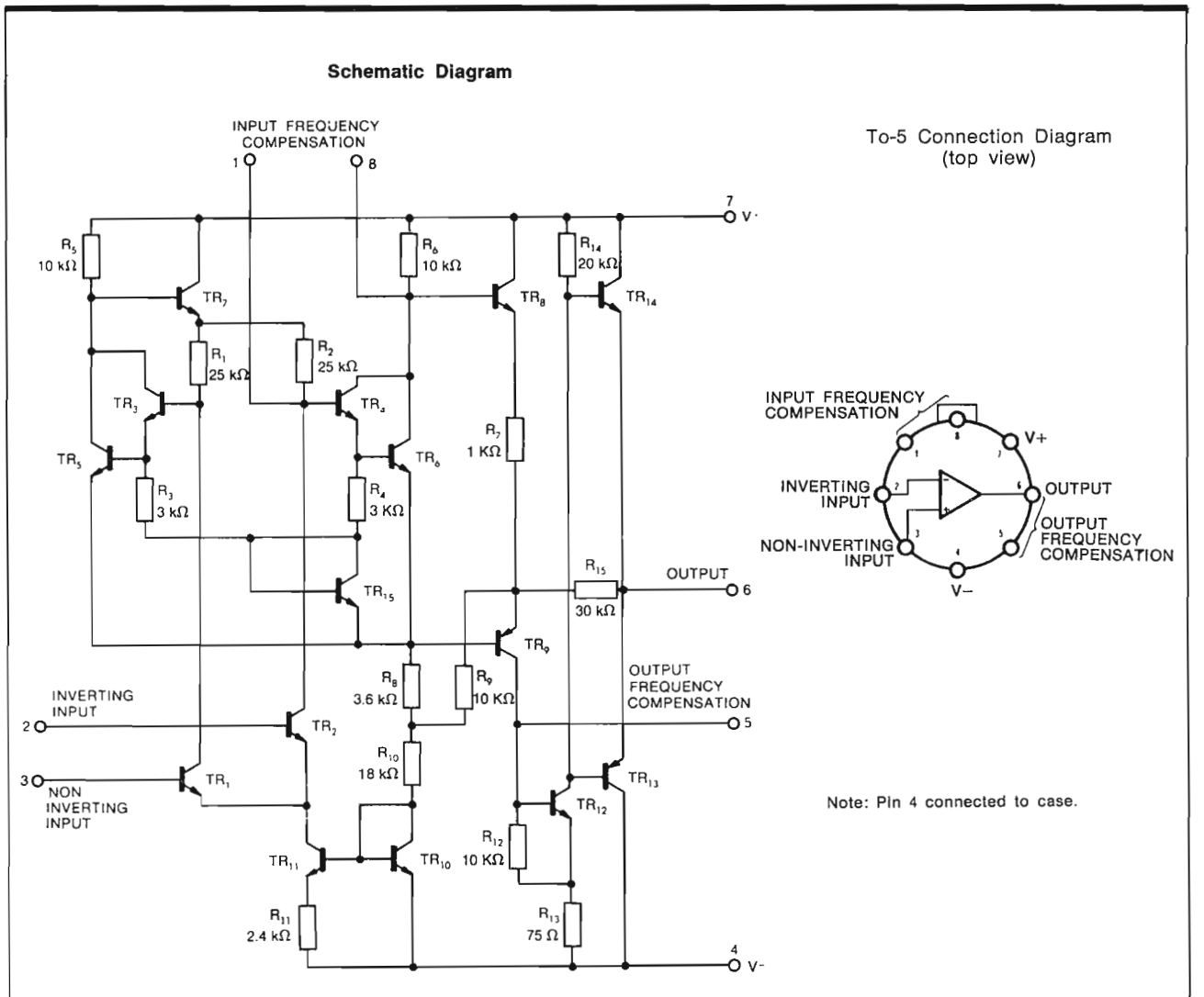


Fig. 2.32 - Complete Circuit of the μA709 Amplifier

As is clear from the figure, it uses the same principle as the input stage current source.

The remaining details of the second stage are that an emitter-follower, TR_7, is used to keep the input stage collector currents out of the collector of TR_5. Additionally, a second emitter-follower, TR_8, is used to prevent loading of the second stage by the output stage.

2.5.4. Output Stage

Level shifting to the output stage, Fig. 2.32, is accomplished using a lateral PNP transistor, TR_9, similar to that described in Section 2.1.2. It is made using what is usually an NPN base diffusion for an emitter. This is surrounded by a second base diffusion which serves as a collector. The normal NPN collector region is then the PNP base. This structure suffers from a rather wide base, displaying a low current gain (approximately 2). However, it has the distinct advantage that it can be made with the standard NPN process with no additional steps or control. The circuit is designed to operate satisfactorily with current gains lower than 0.2, so the device presents no problem in that the PNP will work well enough as long as the junctions are good.

A complementary, class-B output stage is used. The circuit has a built-in dead zone to prevent latch-up or runaway under overload conditions; each output transistor is positively turned off before the other is allowed to conduct. However, a large amount of internal feedback, through R_{15}, is used. This not only gives a low output resistance but also makes the crossover distortion almost indiscernible — even on the open-loop transfer function. An additional advantage of this scheme is that the output stage quiescent current is held to a minimum which helps the design objective of low power consumption.

A vertical PNP transistor is used in the output stage. This device uses the NPN base diffusion for an emitter and the P-type substrate of the integrated circuit for the collector (in the lateral PNP, this PNP action is suppressed by placing the N+ sub-collector diffusion of the NPN underneath it). This PNP has a higher current gain than the lateral PNP but it also presents no problem as far as device yields are concerned since it need only function as a diode to meet circuit requirements.

Although it is not clear from the circuit, the output stage is actually short-circuit-proof. This characteristic is derived from the fact that the output transistors (TR_{14}, TR_{13} and TR_{12}) have small geometries (the whole integrated circuit is about the same size as output transistors that would normally be used). The current gain of these devices is injection-efficiency limited at high current levels. The injection-efficiency-limited current gain is relatively constant for a given process and geometry and falls off at high temperatures so this turns out to be a satisfactory method of short-duration current limiting.

Other details of the output stage are that R_{12} is used to make the circuit insensitive to leakages in TR_9 and TR_{12}. R_{13} reduces the internal loop gain of the output stage to stabilize the internal feedback. The gain of the output stage is essentially determined by the ratio of R_{15} to R_7, independent of the characteristics of the active devices.

2.6 SUMMARY OF μA709 PERFORMANCE

2.6.1 Main characteristics of the μA709 Integrated Amplifier

The typical performance of the μA709 amplifier has been summarised in Table 3. Performance details, such as operating limits, parameters and maximum and minimum ratings can be obtained from the relevant data sheets, available upon request.

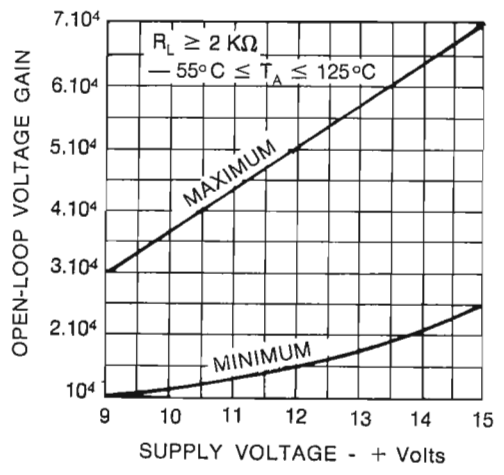


Fig. 2.33 - Voltage Gain as a Function of Supply Voltage

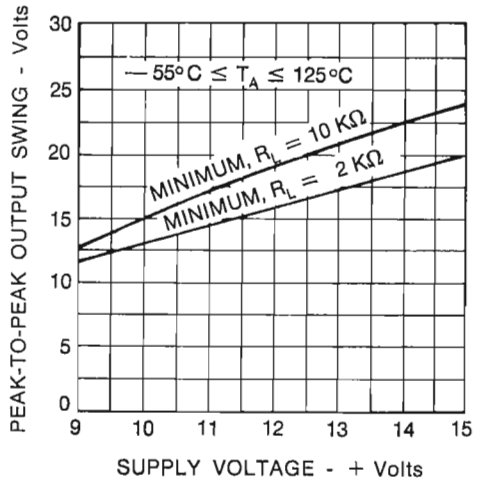


Fig. 2.34 - Output Voltage Swing

The amplifier can operate with a large variety of supply voltages, provided that both negative and positive voltages are kept equal to each other.

The open-loop voltage gain increases with supply voltage V_S, as shown in Fig. 2.33, this represents the maximum and minimum gain as a function of V_S.

Fig. 2.34 shows the minimum values of the maximum output swing which can be obtained with two values of load resistance. Fig. 2.35 and 2.36 show the allowable input common-mode voltage range and the increase of input current with the supply voltage respectively.

Since the transistor current gain increases with temperature, higher input resistance values and lower bias and offset currents are obtainable at high temperatures (see Fig. 2.37, 2.38 and 2.39 respectively).

The amplifier transfer characteristic (Fig. 2.40) shows the linearity and the output voltage swing of the μA709. The « broken » curves represent the high and low temperature transfer characteristics from which it is possible to see how the voltage gain decreases when the temperature increases.

Finally, the maximum output voltage swing as a function of the load resistance is shown in Fig. 2.41. The frequency characteristics and the noise performances of the integrated amplifier are examined separately in Sections 5.3 and 6.3.

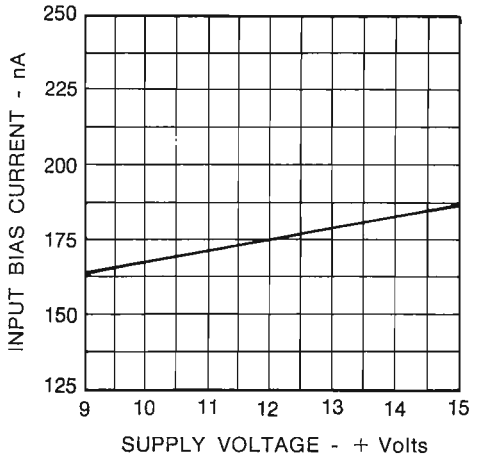


Fig. 2.36 - Input Bias Current as a Function of Supply Voltage

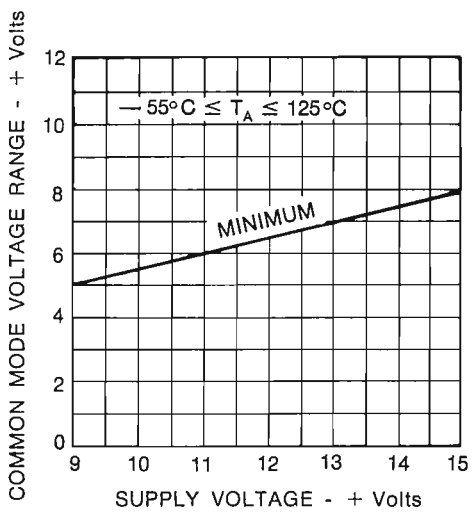


Fig. 2.35 - Input Common Made Voltage Range

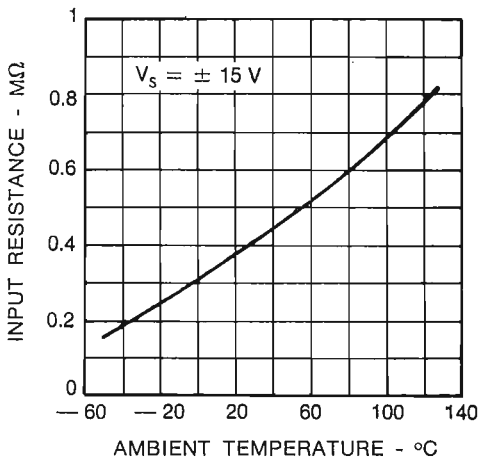


Fig. 2.37 - Input Resistance as a Function of Ambient Temperature

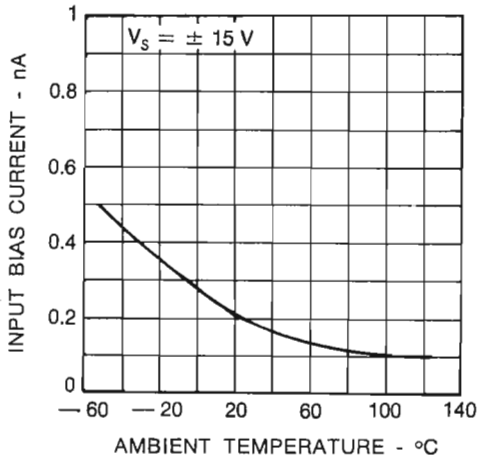


Fig. 2.38 - Input Bias Current as a Function of Ambient Temperature

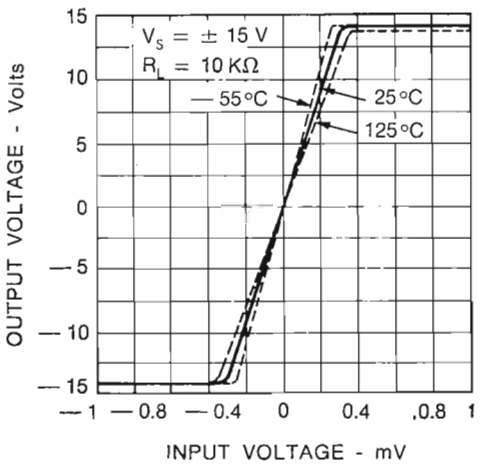


Fig. 2.40 - Voltage Transfer Characteristic

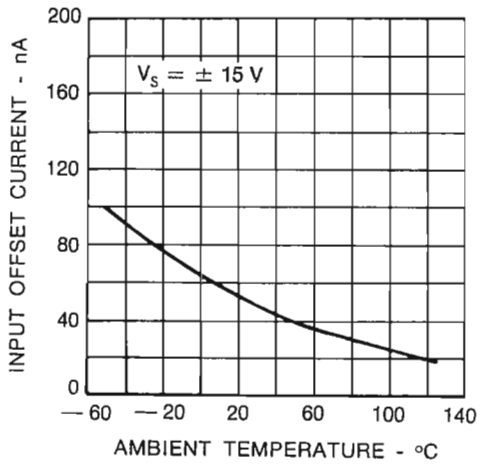


Fig. 2.39 - Input Offset Current as a Function of Ambient Temperature

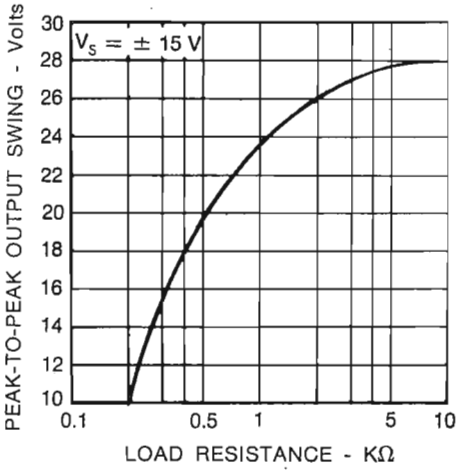


Fig. 2.41 - Output Voltage Swing as a Function of Load Resistance

Typical Conditions: $T_A = 25°C$, $\pm 9\,V \leq V_S \leq \pm 15\,V$ unless otherwise stated

Input Offset Voltage	1 mV
Input Offset Current	50 nA
Input Bias Current	200 nA
Input Resistance	400 kΩ
Output Resistance	150 Ω
Power Consumption	80 mW

The following specifications apply for $-55°C \leq T_A \leq 125°C$:

Large-Signal Voltage Gain	45000
Common-mode Rejection Ratio	90 dB
Input Voltage Range	± 10 V
Supply Voltage Rejection Ratio	25 μV/V
Voltage Drift	3 μV/°C

Table 3 - Typical Performance of μA709 Amplifier

2.6.2 General Circuit Precautions

Use of the μA709 under certain operating conditions can result in abnormal performance or catastrophic failure of the device. Since the source of the problem is not always immediately evident, the most common difficulties are dealt with in the following paragraphs. The protection schemes described may not be necessary in a well-designed system using the μA709, but can be used to good advantage in breadboard and bench work, where accidents are more likely to happen.

LATCH-UP

The common-mode voltage limits of the μA709 are determined for negative inputs by saturation of the current source transistor, and for positive inputs by saturation of the input transistors. Exceeding the positive common-mode limit of the device may cause damage to the inputs through excessive current. Erratic operation can still result, however, even if the current is limited to a safe value. If the transistor on the inverting input saturates, for example, it no longer acts as an inverting amplifier but makes a direct connection between the input and the base of the second stage transistor — thus becoming a non-inverting input. This results in positive feedback, and latch-up will occur if it is possible for the output voltage to hold the input stage in saturation through the feedback network.

This tends to be a particular problem with the voltage-follower circuit of Fig. 2.42. It is easy for a transient to trigger latch-up since the output is connected directly to the inverting input. One possible solution is to put a 33 kΩ resistor between the output and input to limit the feedback current, but this increases the offset voltage. A better method is shown in Fig. 2.43. The output voltage is prevented from rising higher than the common-mode limit (voltage at base of TR_4 - Fig. 2.32, Section 2.5.3) by the diode clamp, D_1. This keeps the input transistor from going into saturation and hence latch-up can-

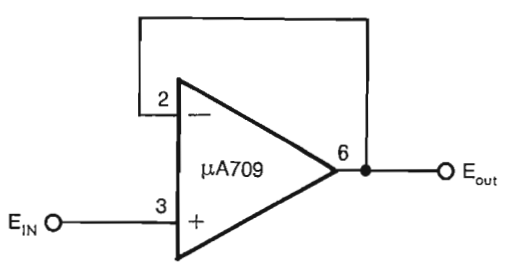


Fig. 2.42 - Voltage Follower

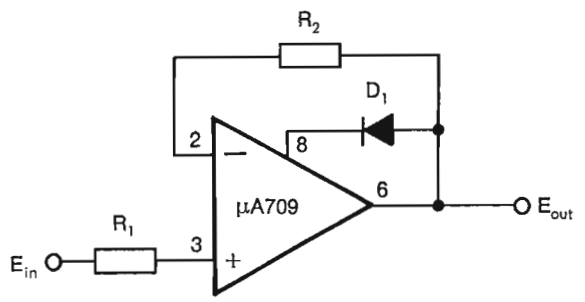


Fig. 2.43 - Protection Against Latch-Up

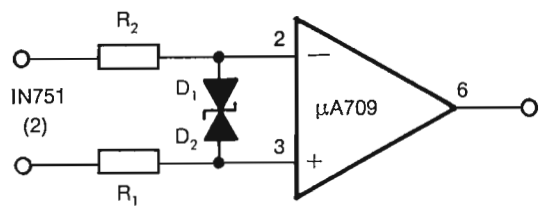


Fig. 2.44 - Protection Against Input Breakdown

not occur. Even though external resistors are not required to prevent latch-up with this circuit, it is wise to include some resistance at each input for protection against differential transients, as discussed subsequently. Up to 10 kΩ can be used without increasing the offset voltage above the guaranteed maximum.

DIFFERENTIAL INPUT VOLTAGE

Although the input common-mode voltage range of the μA709 is a minimum of ± 8 V, the maximum voltage permitted between the inputs is limited to ± 5 V. If one of the inputs is grounded, for example, the other can only be driven as high as + 5 V or as low as — 5 V without exceeding the limit. It is important to observe this maximum rating since exceeding it could cause gross degradation in the input offset current, and input bias current, by drawing excessive current in breaking down the emitter-base junctions of the input transistors. The junctions will short if the current becomes greater than about 50 mA. The circuit can be protected by placing a pair of Zener diodes across the inputs as shown in Fig. 2.44, or a pair of fast silicon diodes as in Fig. 2.45, if the application does not require the full ±5 V differential input voltage range.

Some failures have been traced to the use of ungrounded soldering irons to install the amplifier. Line transients can feed through the insulation of the iron and destroy the unit by arcing over the emitter-base junctions. If the iron is grounded, the circuit grounded or disconnected from any line-operated equipment, and the supply voltages removed, there should be no problem. This type of damage can also be caused by ungrounded test equipment and temperature-chamber transients.

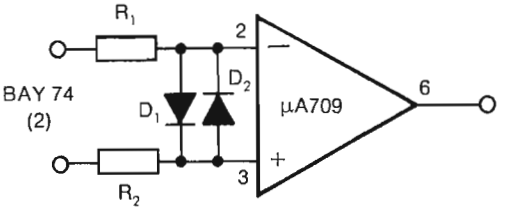


Fig. 2.45 - Protection Against Input Breakdown

SUPPLY VOLTAGE POLARITY

Another point that is sometimes overlooked is the polarity of the power supply voltages. It is quite important that the negative supply terminal always be the most negative point in a monolithic integrated circuit. If the supply voltages are reversed, the isolation diode that normally separates the different elements in the circuit becomes forward-biased. This effectively puts a short between the power supplies, resulting in a large current (greater than 750 mA) that melts the aluminium metallised interconnections. If the possibility exists that the supplies could be reversed, either by accident or by a turn-on transient in the power supply step-up, the amplifier can be protected with a diode as shown in Fig. 2.46.

OUTPUT SHORT-CIRCUIT

As explained in Section 2.5.4, the output stage of the μA709 can withstand a short-circuit for a short period of time. The current gain of the output transistors is injection-efficiency limited at high current levels and falls off at high temperatures. This limits the short-circuit output current to about 75 mA for any condition of input drive. The length of time that the device can survive a direct short is a function of the internal power dissipation and temperature, and is at least 5 seconds at 25°C.

Protection against short-circuits to ground of any duration can be made by inserting a small resistor in series with the output to limit the maximum power dissipation. At the expense of a 10% reduction in maximum output voltage swing (into a 2 kΩ load), the 200 Ω resistor shown in Fig. 2.47 will completely short-circuit protect the amplifier for ambient temperatures to 75°C. The resistor does not affect the normal operation of the circuit since it is inside the feedback loop.

If the μA709 is used to drive logic integrated circuits it is important to limit the maximum output swing of the amplifier, otherwise damage could occur at the input of the logic integrated circuits.

Fig. 2.48 shows a method which effectively overcomes these problems.The diode D_1 prevents negative excursions of the amplifier which exceed approximately — 0.7 V.

The diode D_2 connected to the positive logic supply will prevent the output voltage from becoming greater than the logic supply. Finally, the resistor R_2 in series with the output limits the maximum power dissipation of the μA709.

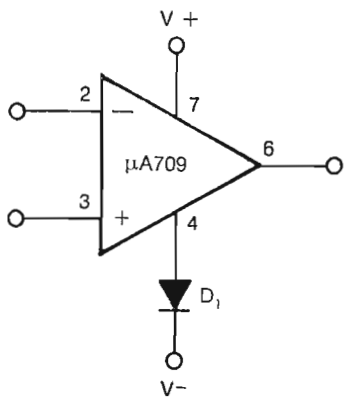


Fig. 2.46 - Protection Against Power Supply Reversal

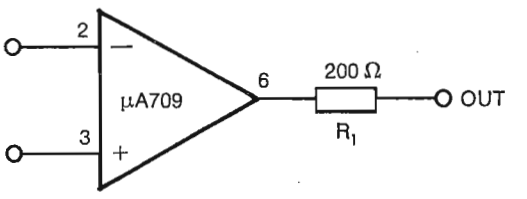


Fig. 2.47 - Protection Against Output Short-Circuit

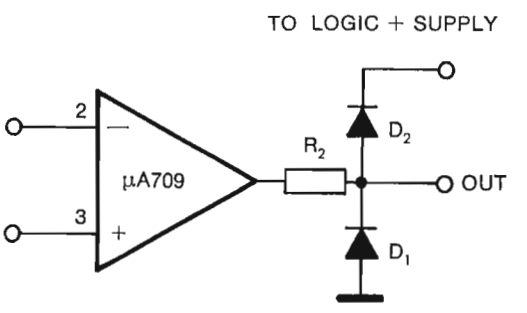


Fig. 2.48 - Logic Compatibility

2.7 DESCRIPTION OF μA710 CIRCUIT OPERATION

2.7.1 Introduction

The μA710 is a high-speed differential comparator whose output has been specifically designed to be compatible with most digital integrated circuit elements. The device is capable of making a voltage comparison with a resolution of 5 mV and a response time of 40 nanoseconds. The circuitry was designed using the philosophies outlined in Section 2.1 and is relatively simple.

The essential function of the unit is to compare a signal voltage with a reference voltage and to produce either a digital on or zero at the output when one is higher than the other. It is useful as a variable-threshold Schmitt trigger, a pulse-height discriminator, a voltage comparator in high-speed analogue/digital converters, a zero crossing detector, or a threshold detector. Units can be combined to form a phase detector, window discriminator, or a core-memory sense amplifier. The comparator features high-speed, low-offset and a large common-mode input voltage operating range.

2.7.2 The Circuit

The comparator, Fig. 2.49, uses a balanced differential input configuration (TR_1 and TR_2) for low offset. The emitters of the input stage are supplied from a current source (TR_9) to make the operating current insensitive to the reference voltage setting. A balanced second stage is also employed, again to keep the offset small: TR_4 is the actual second-stage amplifier, while TR_3 provides biasing for TR_4 and also serves as a unity-gain inverter so that the full differential output of the input stage is delivered to the base of TR_4. Resistors R_1 and R_2 are the collector load resistors for the input stage and R_5 is the collector load resistor for the second stage. TR_5 provides a sink for the input stage collector current and TR_6 is a clamping diode which limits the positive output swing.

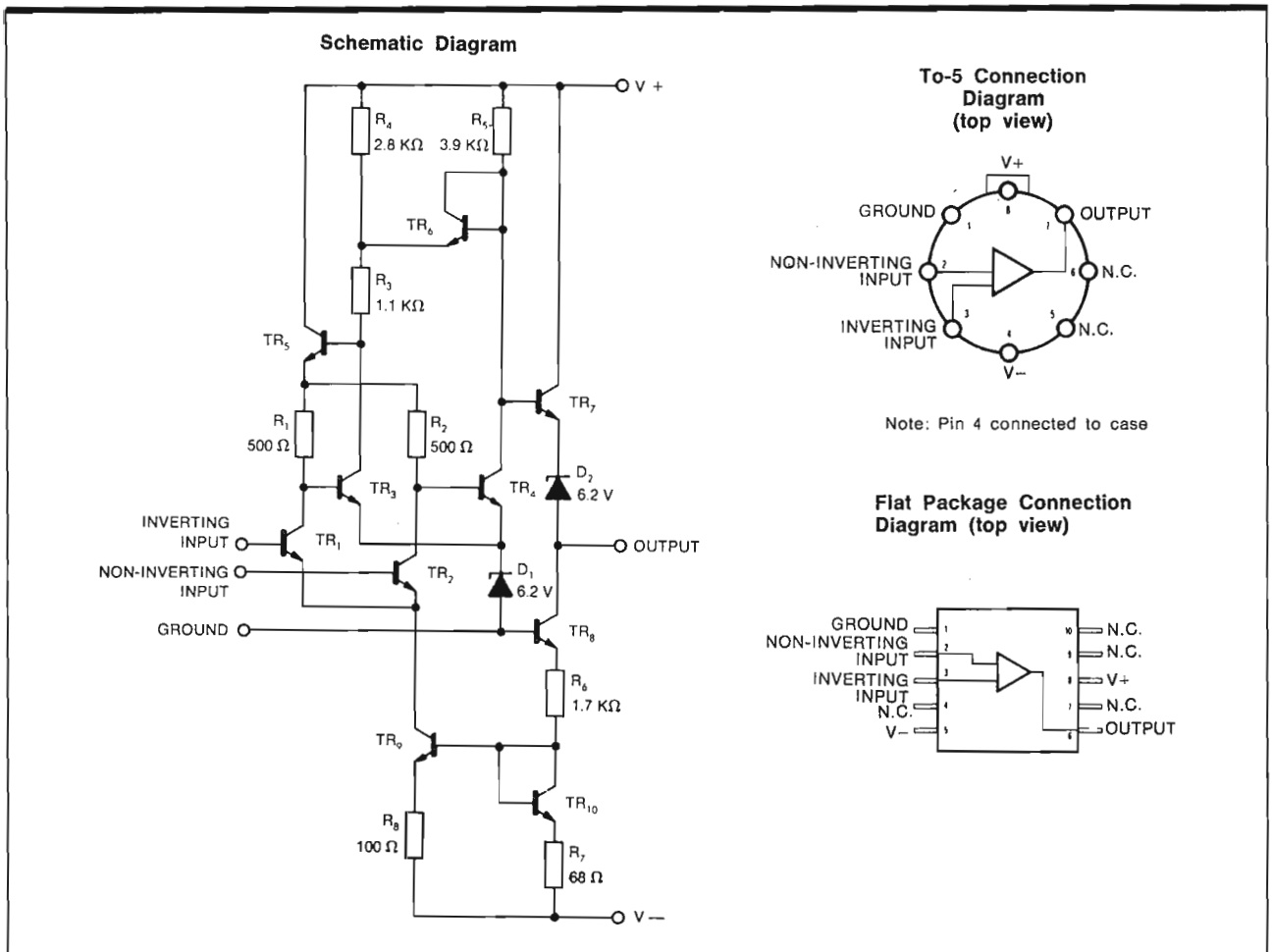


Fig. 2.49 - Circuit Diagram of the μA710

An emitter-follower is used at the output of TR_4 to give a high output current capability. A Zener diode (D_1) in the emitters of the second stage transistors provides a large input voltage range. An identical Zener diode in the output emitter-follower (D_2) level shifts the output back to a level compatible with logic circuits. TR_8 isolates the output from the diode compensated bias divider for the input stage current source.

Using the diode-connected transistor TR_{10}, to compensate for the emitter-base voltage of TR_9 permits the current source to operate with a small voltage-drop across its emitter resistor, R_8. This gives an increased negative input voltage limit.

As can be seen from the foregoing, this voltage comparator is a high-gain differential input, single-ended output amplifier, with provision made to limit the output voltage swing for full compatibility with logic circuitry.

The inherent balance of the circuit and its insensitivity to component values and temperature variation is shown in the following analysis. It is assumed that all the resistors are perfectly matched in ratio, that transistors are perfectly matched and that the Zener diodes are likewise matched. This is a not unreasonable approximation over a broad temperature range using integrated circuit manufacturing techniques. Furthermore, it will be assu-

med that the transistor current gains are sufficiently large so that the base current can be neglected, although a more complete analysis will show that the base currents are insignificant if the transistors are reasonably well matched and the current gain is larger than about 10.

For zero differential input voltage (i.e. signal voltage equal to the reference voltage), the collector currents of TR_1 and TR_2 will be equal since they are identical transistors with the same emitter-base voltages. The collector current of TR_3 can be written as:

$$i_{C3} = \frac{V^+ - V_Z - \frac{1}{2} i_{C9} R_1 - 2V_{BE}}{R_3 + R_4} \quad \ldots\ldots\ldots\ldots\ldots (1)$$

Similarly, the collector current of TR_4 can be written as:

$$i_{C4} = \frac{V^+ - V_Z - V_{BE} - V_{out}}{R_5} \quad \ldots\ldots\ldots\ldots\ldots (2)$$

where V_{out} is the output voltage.

Because of the balanced configuration, these two currents will be equal so:

$$\frac{V^+ - V_Z - \frac{1}{2} i_{C9} R_1 - 2V_{BE}}{R_3 + R_4} = \frac{V^+ - V_Z - V_{BE} - V_{out}}{R_5} \quad \ldots\ldots\ldots\ldots (3)$$

Substituting $R_3 + R_4 = R_5$, in equation (3)

$$V_{out} = V_{BE} + \frac{1}{2} i_{C9} R_1 \quad \ldots\ldots\ldots\ldots (4)$$

It is now necessary to determine the collector current of TR_9. The current in the compensated bias divider for TR_9 is:

$$i_{C10} = \frac{V^- - 2V_{BE}}{R_6 + R_7} \quad \ldots\ldots (5)$$

The collector current of TR_9 will be

$$i_{C9} = \frac{R_7}{R_8} i_{C10}$$

or

$$i_{C9} = \frac{R_7}{R_8} \frac{V^- - 2V_{BE}}{R_6 + R_7} \quad \ldots\ldots\ldots (6)$$

Substituting (6) in (4)

$$V_{out} = V_{BE} + \frac{R_1 R_7}{2R_8} \frac{V^- - 2V_{BE}}{R_6 + R_7} \quad \ldots\ldots\ldots (7)$$

Using the values in Fig. 2.49

$$V_{out} = 0.8V_{BE} + 0.16\,V^- \quad \ldots\ldots\ldots (8)$$

which gives a nominal output voltage of 1.4 V with V = —6 V and zero input voltage.

This is a good choice since the threshold voltage of standard logic circuits is between 0.7 V and 1.7 V.

However, the exact output voltage is only a secondary consideration since the voltage gain of the comparator is quite high (1500) so the difference between a 1.4 V and 0.7 V threshold is only about 0.5 mV at the input.

It can be seen from Equation (8) that the output offset voltage is dependent on the negative supply voltage. However, from the differential of Equation (8),

$$\Delta V_{out} = 0.16\,\Delta V^- \quad \ldots\ldots\ldots\ldots (9)$$

It is evident that a ten-percent change in V^- would give an offset change of 65 μV with a gain of 1500. The sensitivity of offset to production variations of V_{BE} in Equation (8) is in the order of 20 μV, which is totally negligible.

The above analysis has assumed that all resistors are perfectly matched in ratio. In a practical microcircuit, some mismatches are to be expected. Table 4 shows the effect of a ten-percent change in individual resistor values on the input offset voltage. It can be seen that the maching of R_1 with R_2 is by far the most significant, giving a 2.5 mV offset for a ten-percent mismatch. However, matches of about two percent, which would give a 0.5 mV offset, are normally obtained in an integrated circuit. Therefore, the mismatching normally seen does not cause significant unbalance. Similarly, it can be shown that the current-gain mismatches usually obtained do not greatly affect offset, except in the input stage where the offset current is determined by the current-gain match.

Resistor	Nominal Value (Ω)	Change in Offset Voltage (V)
R_1	500	+ 2.4
R_2	500	— 2.4
R_4	3 900	— 0.24
R_5	3 900	+ 0.04
R_6	1 600	+ 0.05
R_7	68	— 0.05
R_8	100	+ 0.05

Table 4 - Change in Input-referred Offset Voltage for a 10% Decrease in Individual Resistor Values.

Finally, the effect of temperature on the output offset voltage (V_{out}) might be considered. From Equations (7) and (8) it can be seen that the only temperature-sensitive parameter is V_{BE}, since resistors hold their initial room-temperature ratios exceedingly well over a wide temperature range. However, it should be noted that this temperature sensitivity is in the right direction to help compensate for the temperature sensitivity of threshold voltage in logic circuits. Since the temperature variations of logic threshold voltage do not have a significant effect on offset, this is not too important; but at least the temperature sensitivity indicated by Equation (8) improves rather than degrades the performance of the comparator.

2.8 SUMMARY OF μA710 PERFORMANCE

2.8.1 Tabulated Performance

Typical performance figures for the μA710 are shown in Table 5. For more details of maximum and minimum tolerances and environmental operating ranges, etc., the appropriate data sheets should be consulted.

In general the μA710C may be used in the circuits described in this Handbook unless it is specifically stated otherwise. Due regard must be made, however, to any closer environmental limits which may be implied. Performance with regard to recovery times and drift will be appropriate to that particular data sheet.

Typical Conditions; $T_A = 25°C$, $V^+ = 12$ V, $V^- = -6$ V

Input Offset Voltage	0.6 mV
Input Offset Current	0.75 μA
Input Bias Current	13 μA
Temperature Coefficient of Input Offset Voltage	3.5 μV/°C
Input Voltage Range	± 5 V
Differential Input Voltage Range	± 5 V
Response Time for 5 mV Overdrive	40 ns
Voltage Gain	1700
Output Resistance	200 Ω
Positive Output Level	+ 3.2 V
Negative Output Level	— 0.5 V
Power Consumption	90 mW

Table 5 - Typical Performance of the μA710

2.8.2 Specification of Operation

The function of comparator, as has been stated, is to produce one digital state at its output when the input signal is above a reference voltage and the opposite digital stage when the input is below the reference. The questions to be answered by a set of specifications, in addition to the usual ones of supply voltage, power dissipation and absolute maximum ratings are:

(a) The accuracy with which the comparator can distinguish between an input signal and the reference signal.

(b) How rapidly the comparator can make the above distinction and what influence the speed of a decision has on accuracy.

(c) The alteration of speed and accuracy caused by different loads being present at the output terminal which the comparator must drive.

The first question can be answered by defining an input offset voltage as the voltage between the comparator input terminals when the output is just at the threshold voltage of the logic (or as the voltage between the input terminals when the logic decision is made at the output).

When the output is at the logic threshold voltage, a very small change in input voltage will cause the output of the logic circuit to swing from zero to a one state. It is not necessary for the comparator output itself to swing from the zero to one state as this does not provide any additional logic output, only more noise immunity. As a matter of fact, when the offset is defined in this manner, the gain of the logic circuit can be added to the gain of the comparator in determining overall gain accuracy. This gives, for example, an equivalent gain of 50 000 when the μA710 is operated with SGS DT L. This combined gain is high enough, with practically all logic circuits, that the voltage gain does not usually need to be considered in determining D.C. accuracy — the offset voltage alone is enough.

The effect of non zero source resistances on the accuracy can be taken into account using the input offset current, when the D.C. resistances seen by the

two input terminals are equal, or the input bias current, when the input resistances are very much different. To prevent the necessity of using worst-case values of offset voltage and offset current, the offset voltage can also be specified for the case where the resistances on each input are equal to or less than a given amount. The use of input resistance to determine loading is not valid with a comparator. The input impedance varies rapidly as the differential input voltage goes through zero and is in excess of a megohm for input voltages greater than two-hundred millivolts.

The second question is a little more difficult. The response time could be defined in many ways. A more or less worst-case situation would be where it is used to accurately determine the amplitude of a large pulse. For example, the situation where a D.C. reference signal (say 0.1 V) is applied to one comparator input and a step function is applied to the other can be considered.

Before the step function is applied, the comparator is completely saturated in one direction (the comparator will actually reach complete saturation with less than 100 mV across the input terminal). Some time after the step function arrives, the comparator output will reach the logic threshold voltage if the step height differs from the reference voltage only by the offset voltage. However, this length of time, in the absence of overshoot, would supposedly be infinite (or at least difficult to determine). Therefore, the response time must be measured with some overdrive in order to have any real meaning. That is, the input step amplitude must be increased by some amount in excess of that required to just barely bring the output from saturation to the logic threshold voltage. The response time can then be defined as the interval between the application of the input step and the time when the output crosses the logic threshold voltage.

The error encountered in making the decision within this period of time is then the amount of overdrive required. For a small overdrive, these parameters will represent a worst-case condition and will be relatively independet of the actual step amplitude as long as it is in excess of 100 mV (smaller step amplitudes will give faster response times since the comparator will not be thoroughly saturated).

The third question, the influence of loading on performance, can be settled by one of two methods: by specifying a maximum output swing and output impedance or, more simply, by specifying maximum fan-out into a known logic system which can be used without affecting performance in other respects.

These parameters do not, of course, completely define the operation of a comparator under all conditions. Others might be the input bias current and input offset current. These will indicate the difference between the effective and actual offset voltages for non-zero source resistances. Knowledge of the open-loop unsaturated voltage gain will enable the effect on offset voltage to be determined for a change in logic threshold voltage.

2.8.3 Description of Performance

The transfer function of the comparator is illustrated in Fig. 2.50. It can be shown that the output voltage swing is compatible with almost all integrated logic forms and that the gain is high enough so that changes in the logic threshold voltage affect accuracy only slightly. The insentivity to temperature over the full Military range is also evident.

Fig. 2.51 and 2.52 give the voltage gain as a function of ambient temperature and supply voltages. The voltage gain increases with the supply voltage whilst decreasing with temperature. Since the current gain of a transistor increases with increase in temperature, lower input bias and offset current are obtained as shown in Fig. 2.53 and 2.54.

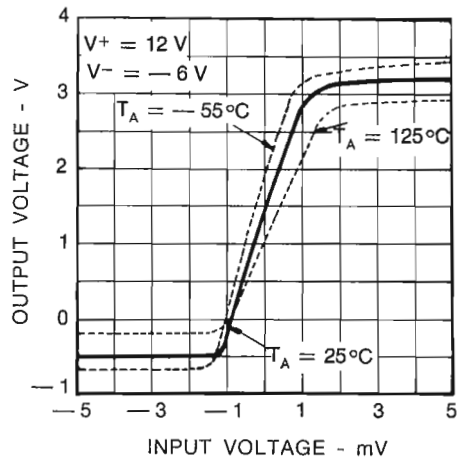


Fig. 2.50 - Voltage Transfer Characteristic

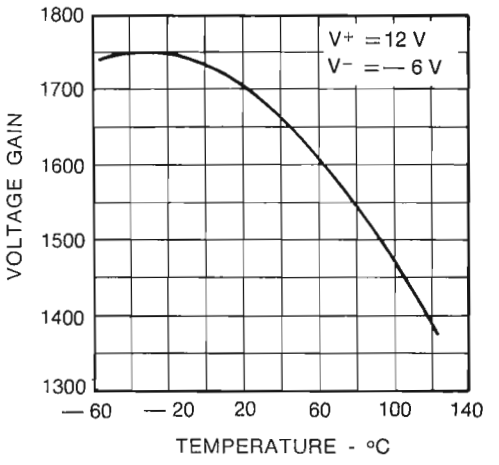


Fig. 2.51 - Voltage Gain as a Function of Ambient Temperature

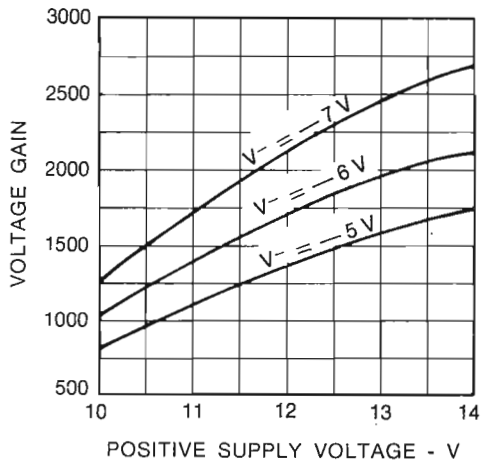


Fig. 2.52 - Voltage Gain as a Function of Supply Voltages

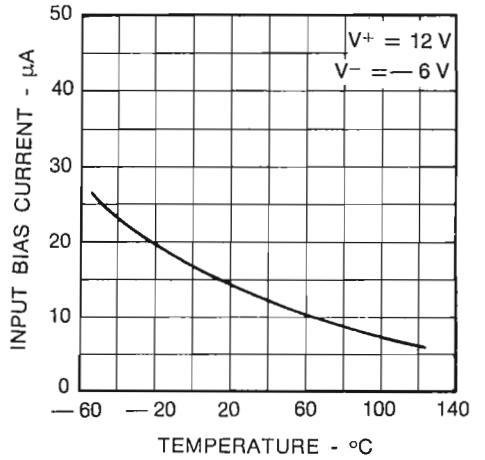


Fig. 2.53 - Input Bias Current as a Function of Ambient Temperature

The fast response of the μA710 is shown in Fig. 2.55 and 2.56. In Fig. 2.55 the comparator is operated with a 0.1 V reference and a positive input step of approximately 0.1 V; the response with 2 mV, 5 mV, 10 mV and 20mV overdrives is given. In Fig. 2.56 a 0.1 V reference and a negative step are used to show the response for positive output.

The curve in Fig. 2.57 shows the frequency response of the comparator operating in the linear region. It is evident that the response time is substantially faster than would be indicated by a first glance at the bandwidth. This happens because the gain at high frequency is still quite large, even though the 3 dB bandwidth is only 4.5 MHz.

The D.C. common-mode rejection of the μA710 is typically 90 dB. What is of much more significance is the common-mode rejection at high frequencies. Fig. 2.58 shows pulse test and its result which demonstrates that the comparator is affected in a negligible way by a fast common-mode signal even in the centre of its active region.

The low offset and drift as shown in Table 5 is proof of the inherent balance of the device. Although the performance is given for only one set of supply voltages, operation is not restricted to these voltages alone. From Equations (1) to (8) (Section 2.7.2) it can be shown that the circuit balance is not seriously affected by the supply voltages. Therefore, satisfactory operation is possible down to about + 10 V and — 4 V. The lower voltage operation will, however, decrease the gain and reduce the positive output level.

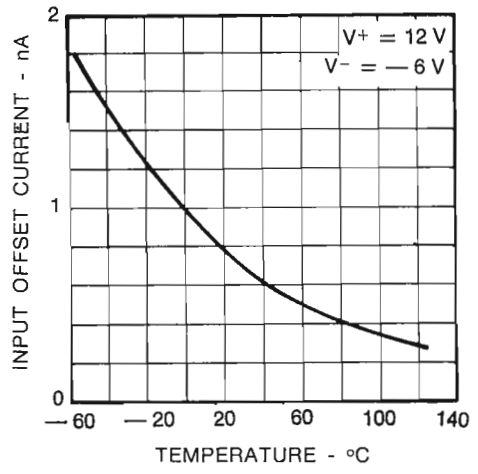


Fig. 2.54 - Input Offset Current as a Function of Ambient Temperature

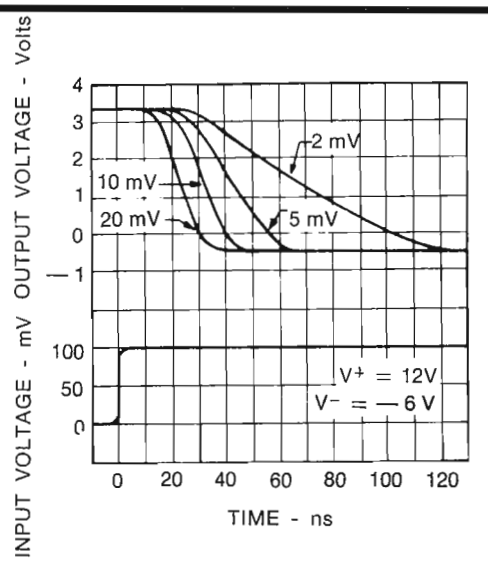


Fig. 2.55 - Response Time for Various Input Overdrives

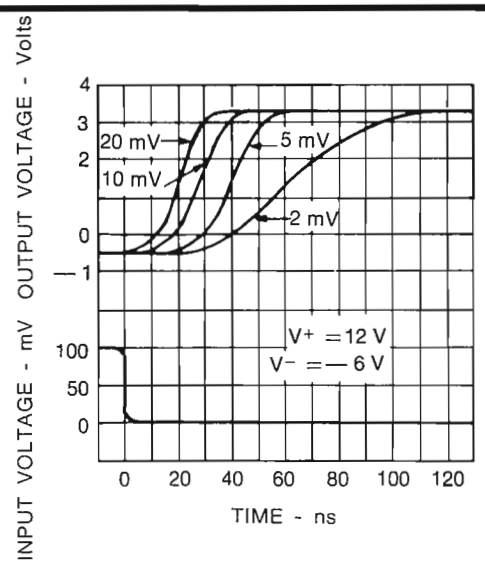
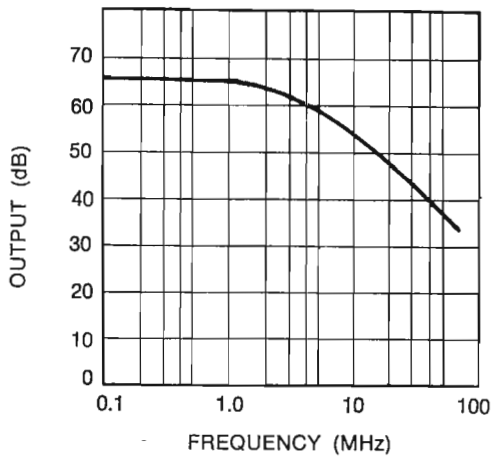
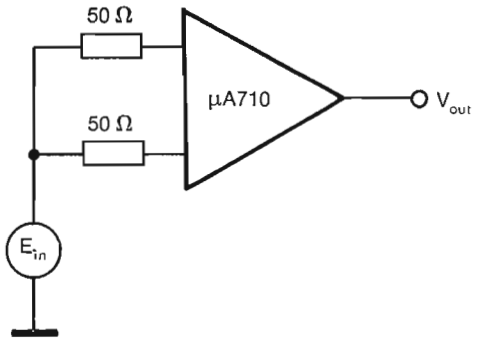


Fig. 2.56 - Response Time for Various Input Overdrives



Rig. 2.57 - Frequency Response of μA710 Linear Operating Range



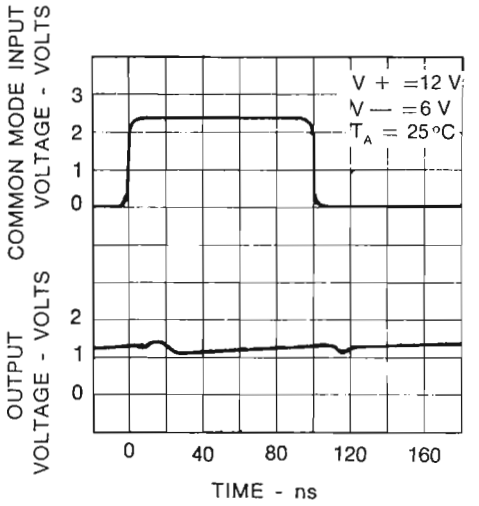


Fig. 2.58 - Common Mode Pulse Response

2.8.4 Logic Compatibility

Specification of logic compatibility can be approached by ensuring that the comparator can drive the logic into full saturation under worst-case conditions. After this is done, it is only necessary to take into account the difference between the threshold voltage of the logic used and the logic threshold specified for the comparator to determine the influence on offset voltage. The effect of differing logic threshold voltages on offset is less than a millivolt with most standard logic circuits so even this can be neglected in the majority of applications.

In general, performance is guaranteed by specification of positive and negative output levels, with and without load, which are compatible with the logic used. The following information is useful in establishing the limitations of the comparator, the circuitry to be used, and the operating conditions under which the comparator is to be specified.

When operated with standard resistor-transistor logic (SGS RT L integrated circuits), the comparator is roughly equivalent to a buffer element and can drive a large fan-out. However, since the comparator operates from a higher supply voltage than a buffer, the internal dissipation with a one-level output can become excessive. In addition, the large output current available from the comparator can overdrive the logic and cause excessive storage. For these reasons, it is advisable to insert a resistor in series with the output of the comparator to limit the current. Recommended values with the μA710 are 1.5 kΩ for a fan-out of one, 510 Ω for a fan-out of two and 270 Ω for a fan-out of three. A small (100 pF) capacitor can be connected in parallel with this resistor to increase the speed of the logic.

Essentially the same rules apply for low-power resistor-transistor logic (SGS MW L). Recommended values of series resistance are 4.7 kΩ for a fan-out of one, 2.2 kΩ for a fan-out of two, and 1.3 kΩ for a fan-out of three. Again, a small capacitor can be added across the resistor for increased speed.

The limiting factor when operating with diode-transistor logic (SGS DT L) is the ability of the comparator to supply the required sink current. The μA710 can drive a DT L fan-out of one, but an external 3.6 kΩ resistor must be added between the output and the —6 V supply for a fan-out of two, and a 2.2 kΩ resistor must be used for a fan-out of three.

With transistor-transistor logic (SGS TT L) the same rules regarding sink current used with DT L must be followed. The high-level, reverse current encountered with TT L can be disregarded because the μA710 is able to supply considerable current in this direction and because the permissible fan-out is low, being restricted by the available sink current.

The μA710 can be used to drive complementary-transistor logic (SGS CT L) directly. The fan-out, however, is limited to one, or perhaps two, by the ability of the comparator to supply the required current at the output high level.

2.9 DESCRIPTION OF μA711 CIRCUIT OPERATION

2.9.1 Introduction

The μA711 is a dual differential voltage comparator constructed on a 0.025 mm² silicon chip; it is designed according to philosophies outlined in Section 2.1. The device features fast response times, low power consumption and compatibility with practically all integrated logic forms. It is intended primarily for core-memory sense applications.

Using the dual comparator, the sense amplifier threshold is determined by external resistors and is practically independent of integrated circuit characteristics. Excellent threshold stability over the full Military temperature range is inherent in the design. Although operating at low power levels, the device is fast enough to work with 0.5 mm. cores. Independet strobing of each comparator channel is provided, and pulse-stretching on the output is easily accomplished. Up to eight sense amplifiers can be OR' ed directly. Finally, the output and strobing are compatible with practically all integrated logic forms.

2.9.2 Device Description

Basically, the function of a comparator is to compare a signal voltage with a reference voltage and produce a digital one or zero at the output when one is higher than the other. The dual comparator described is two independet basic units with the outputs OR'ed. A strobe is provided on each side.

The operation of the comparator can be explained using the simplified circuit of a single side shown in Fig. 2.59. Since the comparator is expected to detect when the voltage on the two input terminals is equal, a differential input stage (TR_1 and TR_2) is used so that the emitter-base voltages cancel when the input is zero. The emitters of the input stage are supplied from a current source (TR_{11}) to make their collector current insensitive to the common-mode input voltage. A balanced second stage is also used: TR_4 is the actual second stage amplifier while TR_3 provides balanced biasing for TR_4. The second stage can be understood by considering that TR_3 and TR_4 are identical transistors. Their bases are fed from a common voltage point through identical resistors (R_1 and R_2). When the input stage collector currents are equal, the collector currents of TR_3 and TR_4 will be equal, so the second stage is balanced. TR_3 also functions as a unity-gain amplifier which inverts the output of TR_1 and combines it with the output of TR_2 at the base of TR_4. A single-ended output is obtained at the collector of TR_4. One feature of the second stage is that under balanced conditions the single-ended output is insensitive to changes in

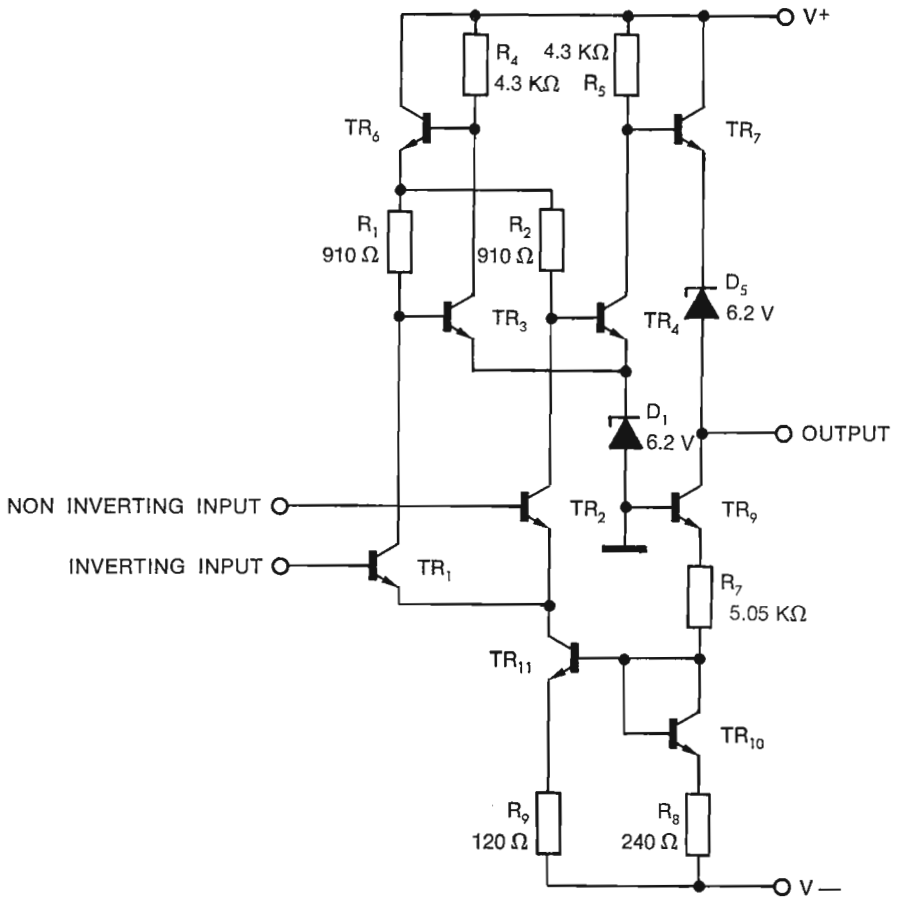


Fig. 2.59 - Simplified Circuit of half the μA711 dual Comparator

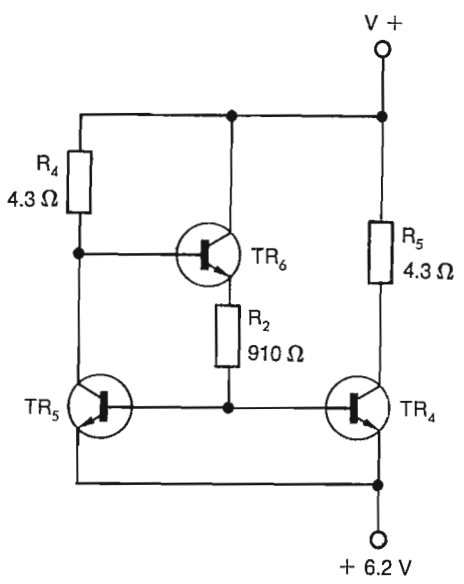


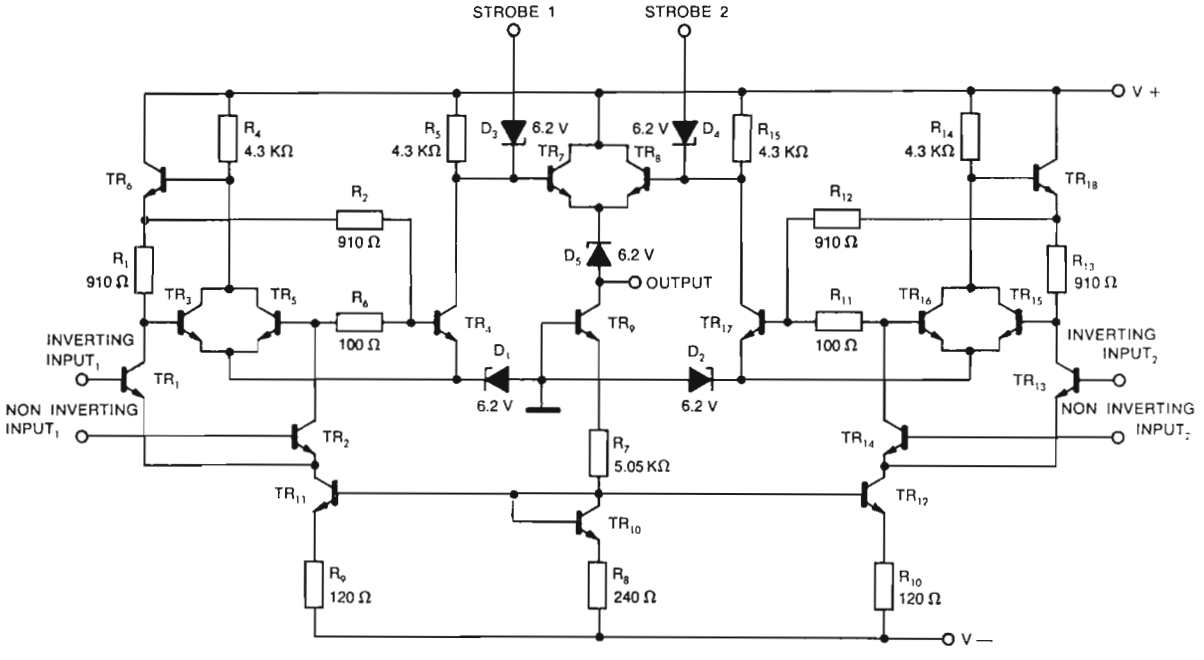
Fig. 2.60- Simplified Circuit Showing Operation of the Saturation Limiter Circuity

positive supply voltage. If the positive supply voltage is increased, the collector currents of both TR_3 and TR_4 will increase such that the voltage on the collector of TR_4 remains constant.

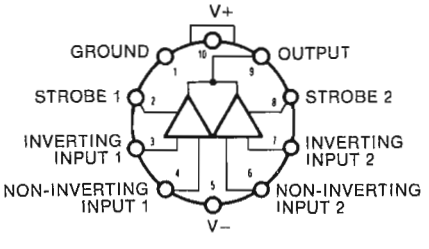
An emitter-follower is used at the output of TR_4 to give high output current capability. A Zener diode (D_1) in the emitters of the second stage transistors provides a large input voltage range (the positive input voltage limit is essentially equal to the voltage on the base of the second stage transistors). An identical Zener diode in the output emitter-follower (D_5) level shifts the output back to a level compatible with logic circuits. TR_9 isolates the output from the diode-compensated bias divider for the input stage current source. Using the diode-connected transistor, TR_{10}, to compensate for the emitter-base voltage of TR_{11} permits the current source to operate with a small voltage drop across its emitter resistor, R_9. This gives an increased negative common-mode limit.

As can be seen from the complete circuit in Fig. 2.61 there is an additional transistor, TR_5. The purpose of this transistor is to reduce the base drive on TR_4 when it saturates. This action not only gives a lower power dissipation but also reduces the storage time of TR_4.

Schematic Diagram



To-5 Connection Diagram (top view)



Note: Pin 5 connected to case.

Fig. 2.61 - Complete Circuit of the μA711 Dual Comparator

When the comparator is operating in the active region, the collector current of TR_2 produces a voltage drop across R_5 which keeps TR_5 in a non-conducting state. Hence, TR_5 does not influence operation in the active region. With a large negative input, TR_2 is turned off and no longer produces this hold-off voltage across R_6, so TR_5 conducts. TR_5 can conduct the entire current through R_4 with only a small voltage drop across R_2 and R_6. Resistor R_1 has a large voltage drop across it since the collector current of TR_1, which is nearly the entire collector current of TR_{11}, is flowing through it. This voltage drop across R_1 cuts off TR_3. This state of operation, with TR_5 conducting and TR_3 cut off, is illustrated in the simplified circuit of Fig. 2.60. Resistor R_6 is eliminated since the voltage drop across it is small enough to be neglected.

If it is assumed that TR_4 and TR_5 in Fig. 2.60 are

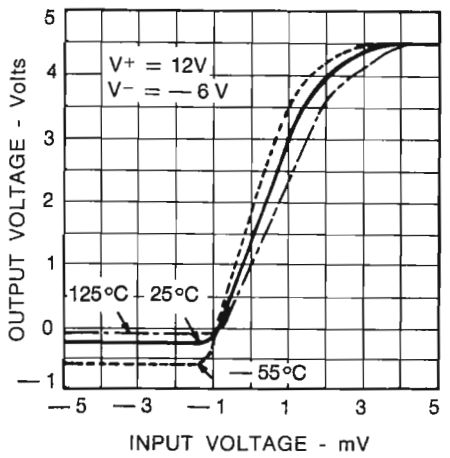


Fig. 2.62 - Voltage Transfer Characteristic

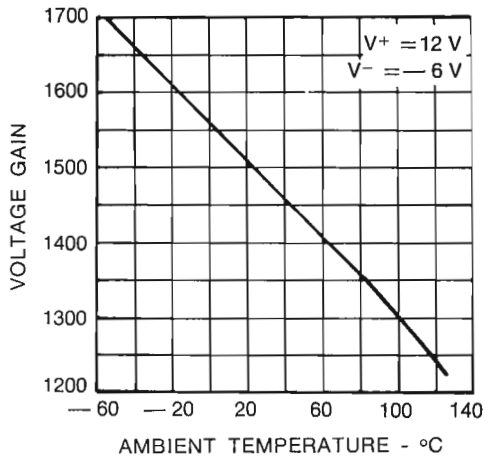


Fig. 2.63 - Voltage Gain as a Function of Ambient Temperature

identical transistors, their collector currents will be equal since they are operating with the same emitter-base voltage. The collector current of TR_5 is determined by R_4 and the voltage drop across it. The collector-to-emitter voltage of TR_5 will be two emitter-base voltage drops (TR_5 and TR_6) plus the voltage drop across R_2, which is small. The collector-to-emitter voltage of TR_4 will be equal to that of TR_5 since their collector currents are equal and R_5 is equal to R_4. However, it is desired that TR_4 should saturate in order to get the proper negative output level. This can be accomplished by making the emitter junction of TR_5 smaller than that of TR_4, so that TR_4 will conduct more current than TR_5 with the same emitter-base voltage (this is easily accomplished in a monolithic integrated circuit). With the proper ratio of device geometries, TR_4 can be made to go just barely into saturation, giving a minimum storage time.

With the dual comparator in Fig. 2.61, the individual comparators are OR'ed at the emitters of the output emitter-followers. Only a single level shifting Zener diode and bias divider are used. Zener diodes on the bases of the output emitter-followers provide independent strobing on each channel: when the strobe on one side is held down to ground level, the output of that side cannot rise. The strobe terminal can also be used to clamp the positive output swing since the output voltage will always be at least one diode drop less than the voltage on the strobe terminal.

2.10 SUMMARY OF μA711 PERFORMANCE

2.10.1 Performance Description

The overall performance of the μA711 is shown in Table 6.

Generally, the μA711C may be used in the circuits described in this handbook unless otherwise specified. Particular care must be taken, however, to observe any close environmental limits which may be implied. For performance concerning the offset and drift, please refer to the relevant data sheet.

The transfer function of the comparator at various operating temperatures is illustrated in Fig. 2.62. This proves that the performance is not greatly effected by temperature. The fact that gain increases at low temperatures and decreases at high temperatures (Fig. 2.63) indicates that the circuit is dependent on the highly predictable transconductance of the transistors rather than current gain. It is also worthwhile to note that the comparator is not designed to have zero output for zero input as is an operational amplifier. Instead, it has an output offset voltage equal to the threshold voltage of common integrated logic circuits. This output offset voltage also has approximately the same temperature coefficient as the threshold of the logic. The fact that the output offset voltage of the comparator matches the logic allows a lower gain with no loss in overall accuracy and permits the gain of the logic circuit to be added to the gain of the comparator in determining overall resolution (this gives an equivalent gain of 50 000 with SGS DT L). This is important since additional gain stages would not only complicate the comparator but also would make it slower.

Conditions: $T_A = 25°C$, $V^+ = 12\ V$, $V^- = -6\ V$

Input Offset Voltage	1 mV
Input Offset Current	0.5 μA
Input Bias Current	25 μA
Temperature Coefficient of Input Offset Voltage	5 μV/°C
Input Voltage Range	± 5 V
Voltage Gain	1 500
Response Time	40 ns
Strobe Release Time	12 ns
Output Resistance	200 Ω
Positive Output Level	+ 4.5 V
Negative Output Level	— 0.5 V
Power Consumption	130 mW

Table 6 - Typical Performance of the μA711 Comparator

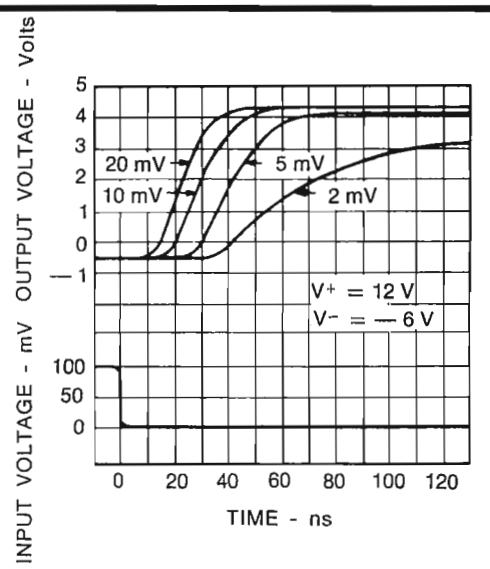


Fig. 2.65 - Response Time for Various Input Overdrives

The voltage gain is also a function of power supply as shown in Fig. 2.64.

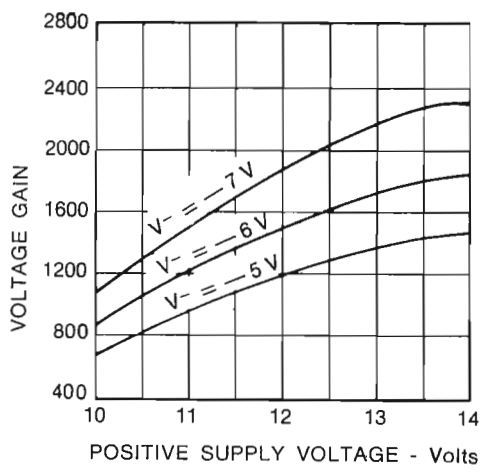


Fig. 2.64 - Voltage Gain as a Function of Supply Voltages

The response time is shown in Fig. 2.65. The input step amplitude is 100 mV and overdrives of 2 mV, 5 mV, 10 mV and 20 mV are shown. The response times are 65 ns, 40 ns, 28 ns, and 20 ns respectively for these overdrives. For smaller input steps, the response time will be somewhat faster for the same overdrive since the internal circuitry of the comparator will not be completely saturated before the pulse is applied. Larger input steps do not materially affect response time since the comparator does not go any deeper into saturation with input voltages larger than 100 mV. Measurement of response time in the manner stated above permits a determination of how much input-referred error is encountered when the comparison is made in a short time interval.

The speed of the strobe circuitry is indicated in Fig. 2.66. The strobe release time is the time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from the zero to the one logic level. The strobe release time is shown for various input conditions in the figure. The 0 mV curve is for an input condition which would put the output at the logic threshold voltage under D.C. conditions. The curve below that is for 1 mV less input voltage and gives an indication of the feedthrough of the strobe pulse when the comparator is barely turned off (it is necessary to wire the comparator into the circuit minimising the stray capacitance between the strobe terminal and the inputs in order to keep this feed-through small). The 2 mV and 5 mV curves represent actual operating conditions and give strobe release times of 14 ns and 10 ns respectively. In these curves, the output does not rise to the maximum output level because of the clamping action of the strobe circuitry when a low amplitude strobe pulse is used. The test conditions shown are representative of the case where the comparator is used with SGS RT L.

Frequently in the design of a sense amplifier where time strobing is used, it becomes necessary to stretch the strobed output pulse of the sense amplifier in order to make it wide enough to be transmitted over a reasonable line length and trigger the storage circuits. The most straightforward way of accomplishing this is to use a one-shot multivibrator, However, the accuracy requirements for the stretched pulse do not warrant going to the complexity of a one-shot. Much simpler methods can be used.

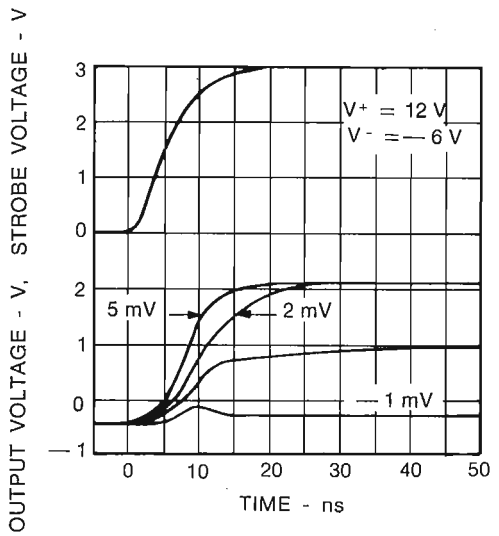


Fig. 2.66 - Strobe Release Time for Various Input Overdrives

Figure 2.67 shows a possible alternative. Loading the comparator with a capacitor on the output will stretch the output pulse. This occurs because the output emitter-follower can charge the load capacitance rapidly, but the output current sink gives a limited rate of discharge. Normally, the strobe width is enough to trigger the logic circuits, and the only fear is that the pulse will be degraded by cable capacitance. However, with the μA711, the capacitances encountered in transmission make the output pulse longer rather than shorter so no discrete capacitor need be used. In the test circuit for Fig. 2.67, an external resistor is connected between the output and the negative supply to give the μA711 a fan-out of one with DT L. This gives considerably less pulse stretching than would be seen with the μA711 alone. It is worthwhile to point out here that the response time and the strobe release time for negative-going outputs were not described previously because they are limited by this pulse stretching characteristic. The negative-going response time up to the base of the output emitter-follower is faster than the positive-going response time because the storage time of the second stage amplifier is not

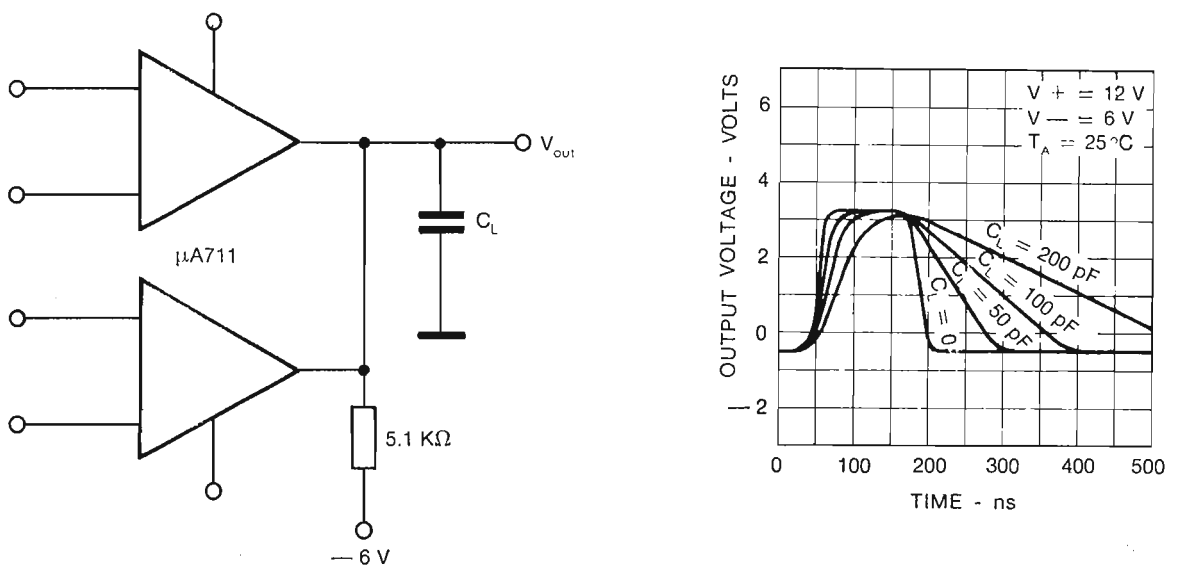


Fig. 2.67 - Output Pulse Stretching With Capacitive Loading

involved. Similarly, the strobe pull-down time is shorter than the release time on the base of the output emitter-follower since a negative-going strobe pulse into the Zener diode will forcibly pull down that point. Therefore, the negative-going response times are limited more by the characteristics of the load than by those of the circuit.

The D.C. common-mode rejection of the μA711 is typically 85 dB. This is considerably more than can be used in a practical high-speed circuit so it is of little interest. What is of much more significance is the common-mode rejection at high frequencies. If this is expressed in terms commonly used in connection with differential amplifiers, it is difficult to interpret for a comparator. However, Fig. 2.68 shows a pulse test and its result which demonstrates that the comparator is affected little by fast common-mode signals even in the centre of its active region. That is, the error encountered due to any reasonable high-frequency, common-mode signals present during comparison is small with respect to the offset voltage and speed resolution. At any time other than when the comparison is being made, common-mode signals can be completely neglected.

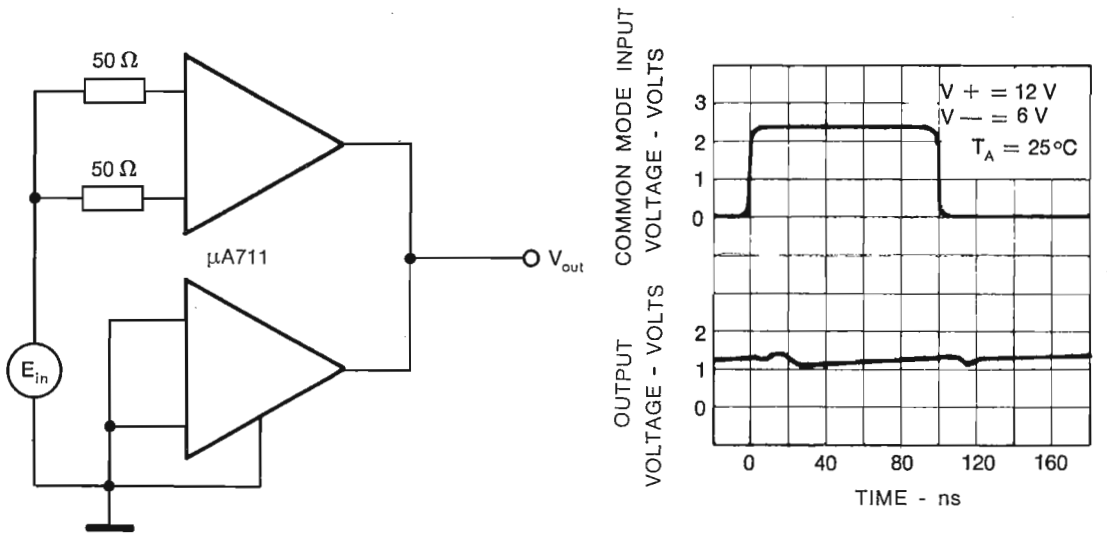


Fig. 2.68 - Common Mode Pulse Response

2.10.2 Logic Compatibility

The output of the μA711 is designed to be compatible with all integrated logic forms. However, because of the substantial differences in the many kinds of logic, it is obvious that the same loading rules used for all these logic families cannot be directly applied to the comparator. Some compromises must be made. In what follows, some of these considerations are discussed.

The output of the dual comparator is designed such that a number of them can be wire OR'ed as is often required in memories. Up to eight devices can be OR'ed, yet the output levels will still be compatible with SGS RT L, DT L and TT L for a fan-out of two.

In order to make possible this OR'ing capability and hold the device dissipation to levels satisfactory for operation over the full Military temperature range, it was necessary to reduce the sink current of the comparator. As a result, at least four devices must be OR'ed before they can provide enough sink current for a DT L fan-out of one. If a single comparator is used to drive a DT L circuit, a 5.6 kΩ resistor must be inserted between the output terminal and the —6 V supply for a worst-case fan-out of one. For a fan-out of two, a 2.4 kΩ resistor must be used. With standard RT L, a single μA711 can handle a fan-out greater than eight. However, even with a fan-out of one, the comparator should not be operated continuously in the positive output state because of excessive power dissipation from the resulting large output current. In the sense amplifier application, this is not a problem because of the low duty-cycle of the positive output condition. However, this excessive output current does increase the storage time of the logic. This can be prevented by inserting a resistor in series with the comparator output. Maximum values for this resistor would be 3.9 kΩ for a worst-case fan-out of one, 1.8 kΩ for a fan-out of two, and 820 Ω for a fan-out of three. A small capacitor can be put across this limiting resistor to increase the speed of the logic. If a number of comparators are wire OR'ed this limiting resistor should be reduced somewhat to compensate for the lower positive output level of the comparator.

The current normally required by the μA711 to strobe down one of the outputs is 1.2 mA. However, if the comparator is in a non-disturbed state, no current is required from the strobe-driving logic since the second stage of the comparator is supplying the current. When a number of comparators are strobed on a common line, only one side of one comparator is likely to be disturbed at any one time. Therefore, it is not necessary that the strobe logic circuitry be able to sink the worst-case current for all the comparators it is driving. As a matter of fact, it is only required that the strobe circuitry be able to sink the worst-case current for one side of one of the comparators.

3. LINEAR INTEGRATED CIRCUIT APPLICATIONS

3.1 μA702A BASIC AMPLIFIER CIRCUITS

3.1.1 Inverting Amplifier (Single-Ended)

With the circuit connected as in Fig. 3.1 the μA702A may be used as a simple single-ended inverting amplifier with a fixed gain dependent on the values of R_1 and R_2.

Assuming an open-loop gain approaching infinity for the amplifier then pin (2) may be considered to be a « virtual earth » since the « non-inverting » input pin (3) is at earth potential.

An expression for the gain with feedback is given by:

$$\frac{V_{in}}{R_1} = \frac{-V_{out}}{R_2}$$

(negative sign due to 180° phase shift inside amplifier)

$$A_f = \frac{V_{uot}}{V_{in}} = \frac{-R_2}{R_1} \qquad \text{..... (1)}$$

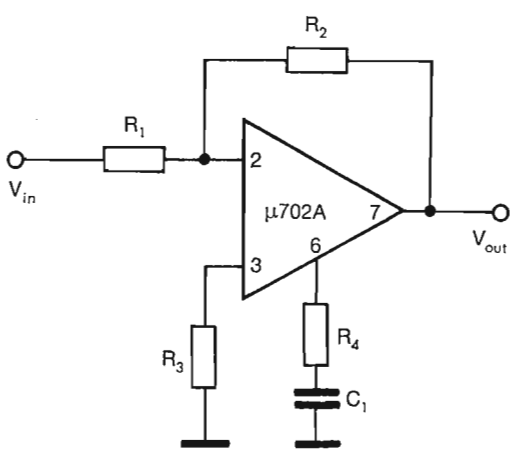


Fig. 3.1 - Inverting Amplifier (Single Ended)

Note (a). R_3 is an optional resistor used to minimise offset voltage and thermal drift. The optimum value is obtained from the expression:

$$R_3 = \frac{R_1 R_2}{R_1 + R_2} \qquad \text{..... (2)}$$

Note (b). R_4 and C_1 are frequency compensating components used to ensure stability of the amplifier. Reference should be made to Section 5 on Frequency Compensation.

Values for a practical amplifier might be:

$R_1 = 2\ k\Omega$	$R_4 = 220\ k\Omega$
$R_2 = 20\ k\Omega$	$C_1 = 910\ pF$
$R_3 = 1.8\ k\Omega$	$A_f = (-)\ 10$

3.1.2 Non-Inverting Amplifier (Single-Ended)

Fig. 3.2 shows the connections for a non-inverting amplifier.

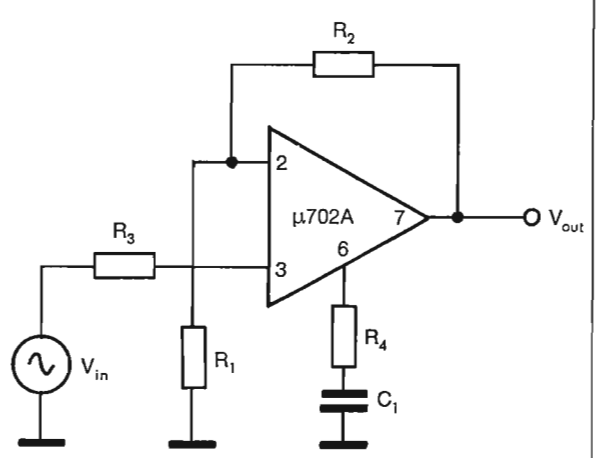


Fig. 3.2 - Non-Inverting Amplifier (Single Ended)

As before, assuming an infinite open-loop gain, then pin (3) and pin (2) always remain at the same potential. An expression for the gain is given by:

$$A_f = \frac{V_{out}}{V_{in}} = \frac{R_1 + R_2}{R_1} \qquad \text{..... (1)}$$

and if $R_2 \gg R_1$ then $A_f \approx \frac{R_2}{R_1}$

Note (a). R_3 is an optional resistor used to minimise offset voltage. See Note (a) of inverting amplifier circuit.

Note (b). R_4 and C_1 are frequency compensating components. Reference should be made to section 5 for optimum values.

Values for a practical amplifier might be:

$R_1 = 1\ k\Omega$	$R_4 = 1\ k\Omega$
$R_2 = 51\ k\Omega$	$C_1 = 220\ pF$
$R_3 = 910\ \Omega$	$A_f \approx 50$

3.1.3 Differential Input Amplifier (Single-Ended)

With the circuit shown in Fig. 3.3 the μA702A may be used as a differential input, single-ended output amplifier.

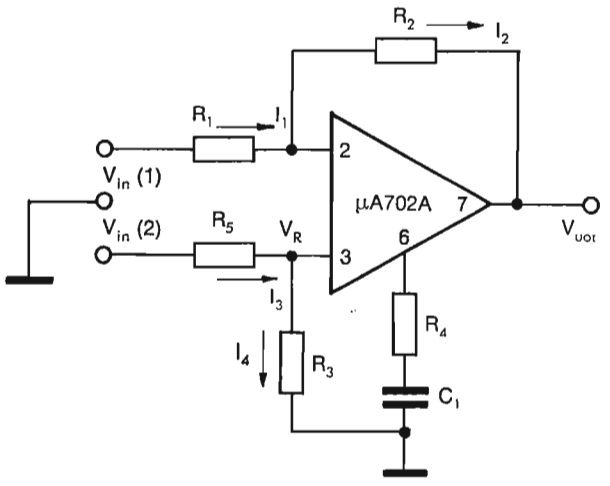


Fig. 3.3 - Differential Input Amplifier (Single Ended)

Assuming infinite open-loop gain and infinite input impedance, then pins (2) and (3) will be at the same common-mode input voltage V_R.

An expression for the gain may be obtained as follows:

The current in the upper loop are equal and also in the lower loop (since no current flows into pins (2) or (3), i.e. $i_1 = i_2$ and $i_3 = i_4$).

$$V_{out} = V_R \cdot \frac{R_1+R_2}{R_1} - \frac{R_2}{R_1} V_{in(1)} \qquad \ldots\ldots\ (1)$$

$$\text{But } V_R = V_{in(2)} \cdot \frac{R_3}{R_5+R_3} \qquad \ldots\ldots\ldots\ (2)$$

$$V_{out} = V_{in(2)} \cdot \frac{R_3}{R_5+R_3} \cdot \frac{R_1+R_2}{R_1} - V_{in(1)} \frac{R_2}{R_1} \qquad \ldots\ldots\ (3)$$

Note (a). If $R_1 = R_5$
$R_2 = R_3$

Equation (3) simplifies to:

$$V_{out} = (V_{in(2)} - V_{in(1)}) \frac{R_2}{R_1} \qquad \ldots\ldots\ (4)$$

Note (b). The common-mode rejection ratio (CMRR) of this amplifier, (S) is also a function of resistance tolerance. Therefore:

$$\frac{1}{S} = \frac{1}{H} + \frac{1}{S_A}$$

where S_A is the CMRR of the μA702A and H is the rejection factor of the external resistance bridge and is given by:

$$H = \frac{R_1+R_2}{R_1} \cdot \frac{2}{\dfrac{(R_1-R_5)}{R_5} - \dfrac{(R_2-R_3)}{R_3}}$$

Note (c). C_1, R_4 are for frequency compensation. Values for a practical amplifier might be:

$R_1 = 2\ k\Omega$ $\quad$ $R_5 = 2\ k\Omega$
$R_2 = 100\ k\Omega$ $\quad$ $C_1 = 220\ pF$
$R_3 = 100\ k\Omega$ $\quad$ $A_f = 50$
$R_4 = 1\ k\Omega$

Resistor tolerances should be 0.5%.

3.1.4 High Input Impedance D.C. Amplifier

The circuit shown in Fig. 3.4 may be used when a high input impedance D.C. amplifier is required.

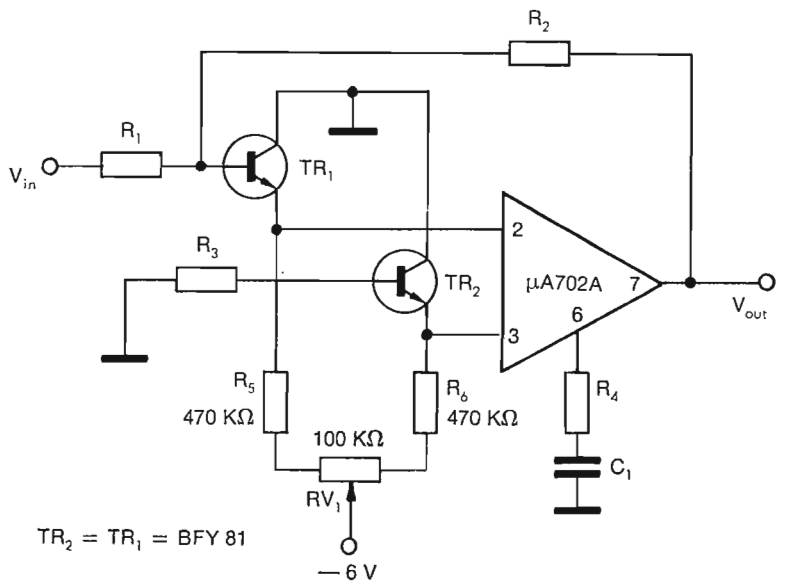


Fig. 3.4 - High Input Impedance D.C. Amplifier

The useful common-mode operating range would be from between approximately —4 V to 0 V with this configuration.

The expression for gain is given by:

$$A_f = \frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1} \qquad \text{..... (1)}$$

TR_1 and TR_2 (BFY81) is a dual transistor device having high gain at low current and closely matched V_{BE} and $V_{BE}/^{o}C$ characteristics.

Note (a). R_4 and C_1 are used for frequency compensation and their optimum value will depend on the amplifier gain. (See Section 5).

Note (b). With the common collectors of the BFY81 returned to earth, it is not necessary to provide protection against a latch-up condition since, before the input exceeds a maximum permissible positive value, the base-collector junction will become forward biased.

Note (c). If it is required to operate about earth potential, the common collectors may be returned to the positive line but the remarks in Note (b) will not be applicable.

Note (d). For minimum output offset

$$R_3 = \frac{R_1 \; R_2}{R_1 + R_2}$$

Note (e). RV_1 provides a method for compensating for the input offset voltage (see 3.1.7).

3.1.5 High Input Impedance A.C. Amplifier

In order to provide a high input impedance amplifier, the circuit of Fig. 3.5 may be used. This employs a « bootstrap » configuration giving positive feedback from the output to the non-inverting input pin (3).

The approximate expression for the input impedance is:

$$R_{in} \approx \frac{A_{vo}}{A_f} \cdot R_A \quad \text{where } A_{vo} = \text{Open-loop voltage gain}$$

A_f = Gain with feedback

R_A = Input impedance into pin (3)

With typical values of $A_{vo} = 2\,000$

$R_A = 10\ k\Omega$

If $A_f = 10$ then $R_{in} = 2\ M\Omega$

A_f is given by expression $A_f = \dfrac{R_1 + R_2}{R_1}$

Note (a). R_4 and C_4 provide frequency stability. Reference should be made to Section 5 for optimum values.

Note (b). R_3 provides thermal stability and is given by $R_3 + R_1 \approx R_2$.

A practical amplifier might have the following values:

$C_1 = 1\ \mu F$	$R_1 = 10\ k\Omega$
$C_2 = 1\ \mu F$	$R_2 = 91\ k\Omega$
$C_4 = 910\ pF$	$R_3 = 82\ k\Omega$
$A_f \approx 10$	$R_4 = 220\ \Omega$

3.1.6 Low-Noise, High Input Impedance Amplifier

Fig. 3.6 shows a circuit suitable for a low-noise preamplifier for use as a low-level audio or instrumentation transducer amplifier. A matched pair of low-noise transistors is used as a differential input stage to provide good common-mode rejection and

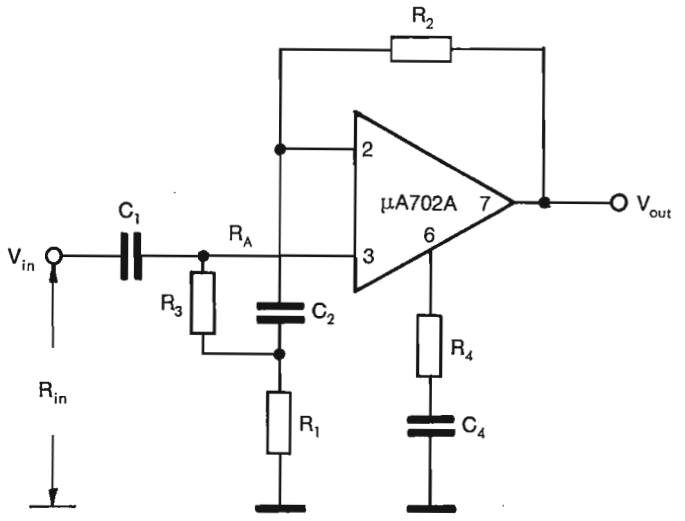


Fig. 3.5 - High Input Impedance A.C. Amplifier

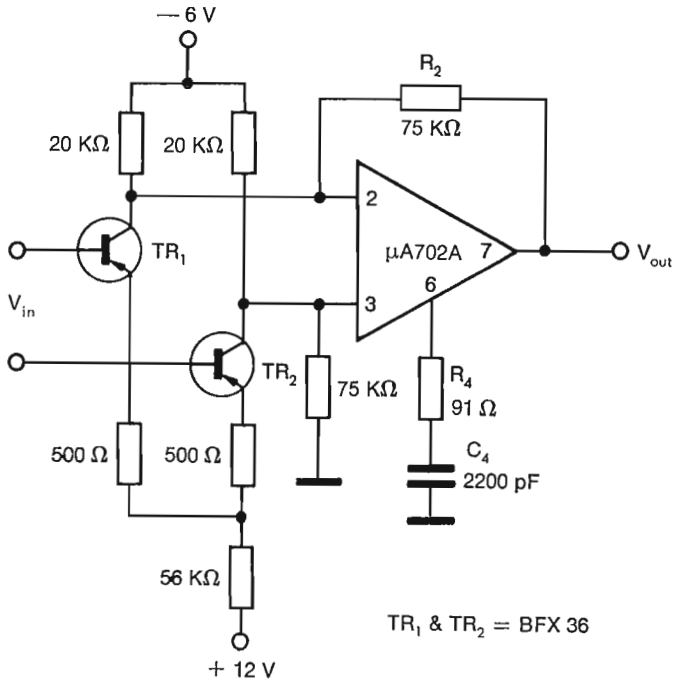


Fig. 3.6 - Low Noise, High Input Impedance Amplifier

high input impedance. Overall feedback is not employed but a reasonably constant gain of 100 is obtained.

A particular advantage of this input configuration is an increased common-mode operating range in the positive direction compared with that of the μA702A alone. Good rejection of unwanted induced noise in the input leads is also provided.

Note: C_4 and R_4 are for frequency stabilization.

3.1.7 Voltage-Follower

The restricted positive-going, common-mode operating range of the μA702A limits the allowable peak-to-peak input swing when the amplifier is used in a unity gain non-inverting configuration. Fig. 3.7 shows a circuit where this restriction is overcome by « bootstrapping » the earth point pin (1) directly to the output. This prevents either input terminals of the amplifier from becoming significantly positive with respect to pin (1).

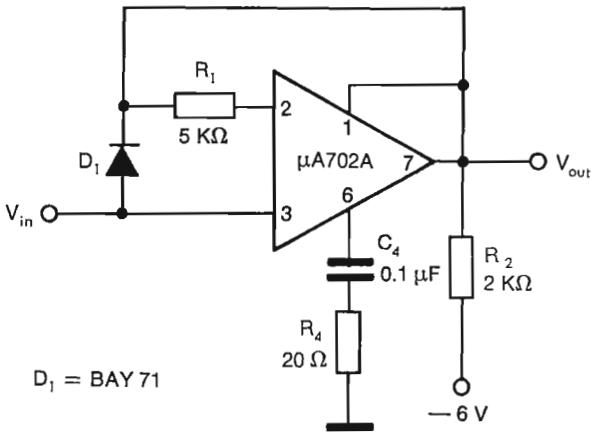


Fig. 3.7 - Voltage Follower

R_2 is an optional resistor which extends the possible peak negative output swing where the amplifier is heavily loaded.

Using supplies of +12 V and —6 V will enable a +3 V signal to be handled.

Note (a). C_4 and R_4 provide frequency compensation
Note (b). D_1 protects the input from latch-up.

3.1.8 Amplifiers with Frequency Compensation

For detailed examination of the criteria for the design of frequency compensation, reference should be made to the appropriate Section 5. Fig. 3.8 (a) and (b) depict two of the most useful basic circuit configurations.

Using the design equation for the circuit of Fig. 3.8 (a):

$$R_4 = 20\left(1+\frac{R_1}{R_2}\right)\Omega \qquad \ldots\ldots (1)$$

Power supplies at +12 V and —6 V

$$C_4 = \frac{0.01}{1+\frac{R_1}{R_2}}\ \mu F \qquad \ldots\ldots\ldots (2)$$

This will give maximum bandwidth with adequate stability margin for most applications.

Note that decreasing the value of R_4 and increasing C_4 improves the stability margin further, but reduces the bandwidth of the amplifier. This compensation technique does not allow the full peak-to-peak output swing of the amplifier to be used. When this is important, then the type of circuit in Fig. 3.8 (b) should be used.

Here the compensation is placed across the input terminals and the optimum values are given by:

$$R_5 = 5R_1\ \Omega \qquad \ldots\ldots\ldots\ldots (3)$$

Power supplies at +12 V and —6 V

$$C_5 = \frac{0.04}{R_1}\ \mu F \qquad \ldots\ldots\ldots (4)$$

where R_1 is in kilohms.

Note (a). Special techniques using pin 5 are described in Section 5 (Frequency Compensation).
Note (b). In general, circuits employing the μA702A, where the open-loop gain is > 2 000 and there is more than approximately 20 dB of feedback, will require some form of frequency compensation to ensure unconditional stability.

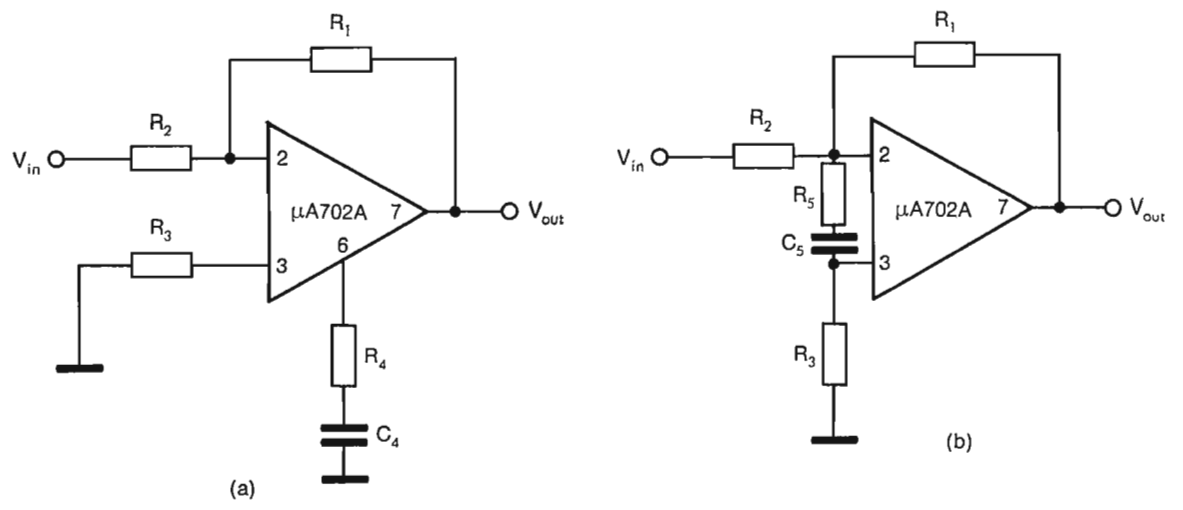


Fig. 3.8 - Amplifiers with Frequency Compensation

3.1.9 Amplifiers with Offset Voltage Balancing

The steady-state voltage present at the output of the μA702A when used as a simple amplifier will not, in general, be exactly zero for the condition of no input D.C. signal. The reasons for this are:

(a) Mismatch of the electrical characteristics within the amplifier, predominantly due to the difference in V_{BE} and h_{FE} of the input stage differential pair and also the mismatch of their associated collector resistors.

(b) Finite input current flowing through the series resistors in the input leads.

Since the magnitude of this output offset voltage will also be dependent upon the loop gain of the circuit, it is convenient to refer its value back to the input and define it as follows:

Input offset voltage is that voltage which must be applied between the input terminals to obtain zero output voltage.

To obtain the total value of the offset voltage, it is necessary to take into account the voltage due to the product of input terminal current times the input series resistance. Since the μA702A has a differential input, it is generally possible to arrange that the impedance from the inverting and non-inverting pins to ground is approximately equal, thus the effect of the input bias current through the input resistors is self-cancelling.

The difference between the input currents is defined as the input offset current. It is clearly the value of this multiplied by the input resistance which will contribute to the total input voltage offset.

For D.C. - coupled amplifiers, it is often desirable to be able to cancel out the input offset by means of some independent circuit so that, for example, there is a zero output when a bridge transducer at the input is in a balanced condition.

Less obviously, for an amplifier having A.C. coupling at the output and especially if it has high gain input source resistance, then the undistorted peak-to peak output swing may be seriously restricted if the steady state output voltage is already appreciably unbalanced.

The best type of circuit chosen to balance the input offset voltage depends generally on the signal source impedance. For low impedances, i.e., below 2 kΩ then the circuits shown in Fig. 3.9 (a) and (b) are suitable. For a high impedance source acting as a current generator, then Fig. 3.9 (c) would be better.

Note (1). To obtain reasonable control for worst-case conditions then, for the circuit of Fig. 3.9 (a) the potentiometer chain and R_4 should be so chosen such that:

$$R_4 \gg R_1$$

and if the maximum current that can be delivered via R_4 is I_b $R_1 \approx 10$ mV.

Note (2). For circuit Fig. 3.9 (b)

$$RV_1 \gg R_1 \text{ and } \frac{R_4 \cdot V^-}{R_5} \approx 10 \text{ mV}$$

Note (3). For circuit Fig. 3.9 (c)

$$(RV_1 + R_1)\ \min \approx \frac{R_2}{2}$$

$$(RV_1 + R_1)\ \max \approx 2R_2$$

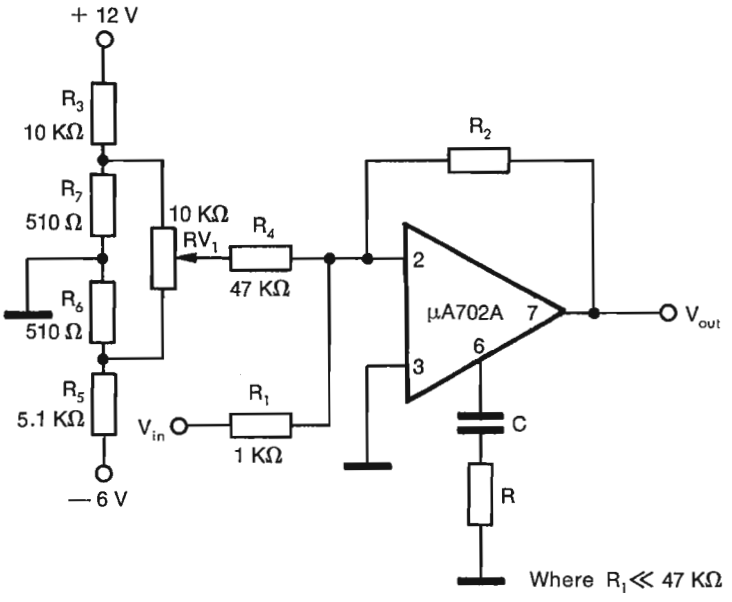


Fig. 3.9 (a) - Offset Voltage Balancing

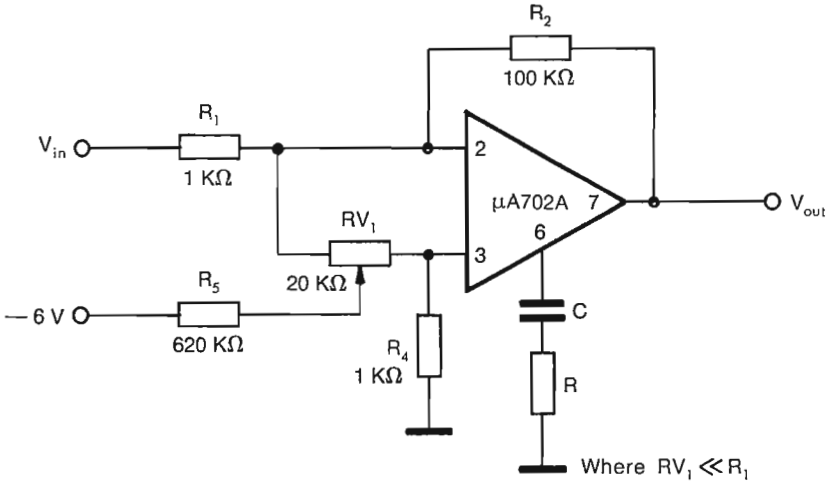


Fig. 3.9 (b) - Offset Voltage Balancing

3.1.10 High Output-Current Amplifier

In some cases the output characteristics of the μA702A may not be adequate (A buffer stage can be used to boost the current output capability and reduce the output impedance at the same time).

Fig. 3.10 shows the amplifier circuit diagram using a μA702A followed by a common-collector complementary symmetry stage able to deliver an output current of 50 mA into a 100 Ω load.

In this circuit the μA702A and transistors TR_1 and TR_2 are protected against a permanent short-circuit of the output by use of resistors R_5 and R_6 and current-limiting resistors R_9 and R_{10} respectively. Moreover, resistors R_5, R_6, R_7 and R_8 are chosen to allow an output swing of ±5 V.

A voltage supply of ±12 V is used for the amplifier, which has a closed-loop gain of 50, the voltage supply of —6 V for the μA702A is obtained by means of Zener diode Z_1.

Note (1). C_1 and R_4 provide frequency compensation.

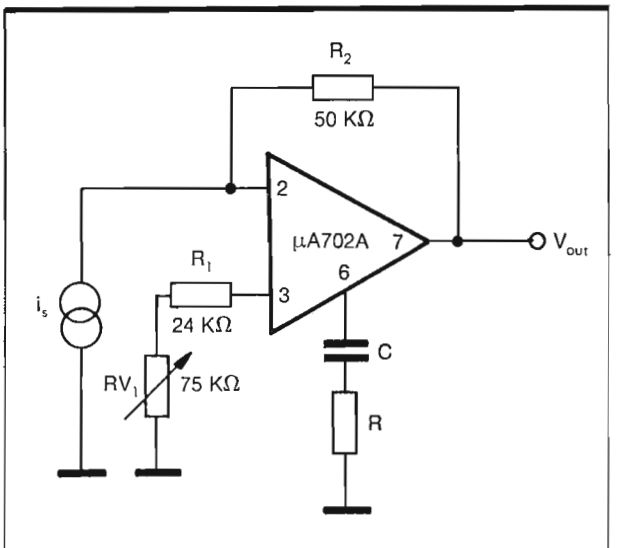


Fig. 3.9 (c) - Offset Voltage Balancing (Current Source)

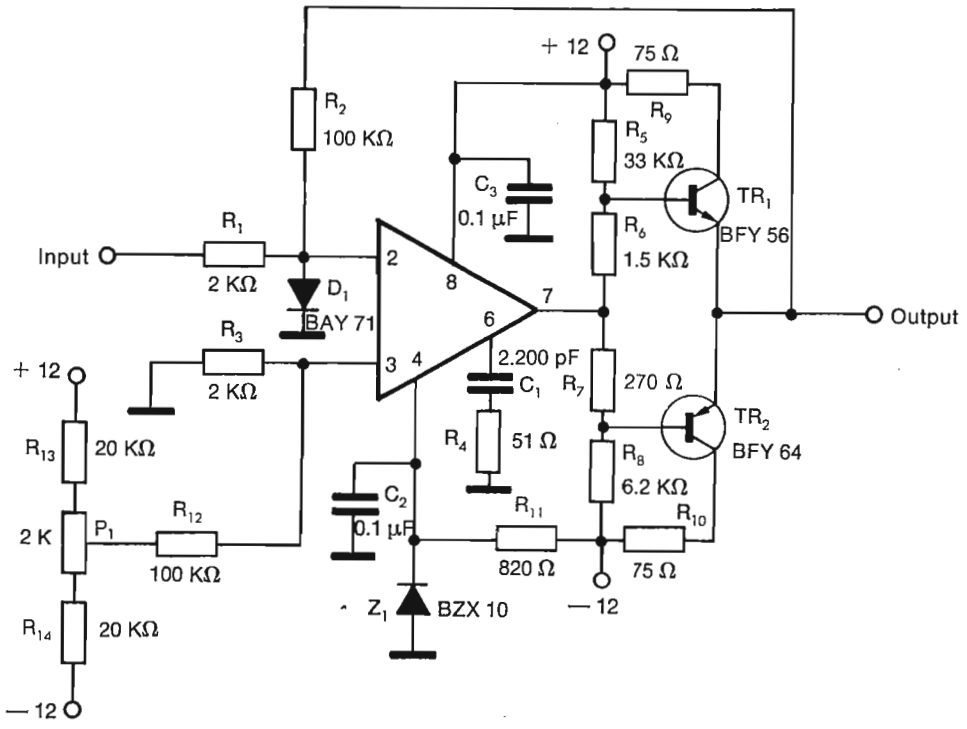


Fig. 3.10 - High Output Current Amplifier

Note (2). D_1 prevents input latch-up. (See Section 2.4.2)

Note (3). Potentiometer P_1 is used to set the offset to zero.

3.1.11 Low-Pass Amplifier

Fig. 3.11 shows the circuit for a low-pass amplifier. The D.C. gain of this circuit is given by:

$$A_{DC} = \frac{-R_2}{R_1}$$

The 3 dB attenuation frequency is given by:

$$f = \frac{1}{2\pi R_2 C_2}$$

Since the relationship between the input and output is:

$$V_o = -V_{in}\frac{R_2}{R_1} \cdot \frac{1}{1+R_2C_2S}$$

(where S is the operator e.g., $j\omega$).

Note (1). C_1 provides frequency stabilization (see Section 5).

Also $C_1 \gg \frac{C_2}{10}$ (see Section 2.4.2).

Note (2). C_3 eliminates the effect of input capacitance at pin (3).

Note (3). R_3 minimises the output offset voltage. Reference should be made to appropriate Section.

Note (4). Diode D_1 protects against possible input latch-up (see Section 2.4.2).

Values for a typical circuit might be:

$R_1 = 50\ k\Omega$	$C_1 = 0.1\ \mu F$
$R_2 = 50\ k\Omega$	$C_2 = 1\ \mu F$
$R_3 = 25\ k\Omega$	$C_3 = 0.1\ \mu F$

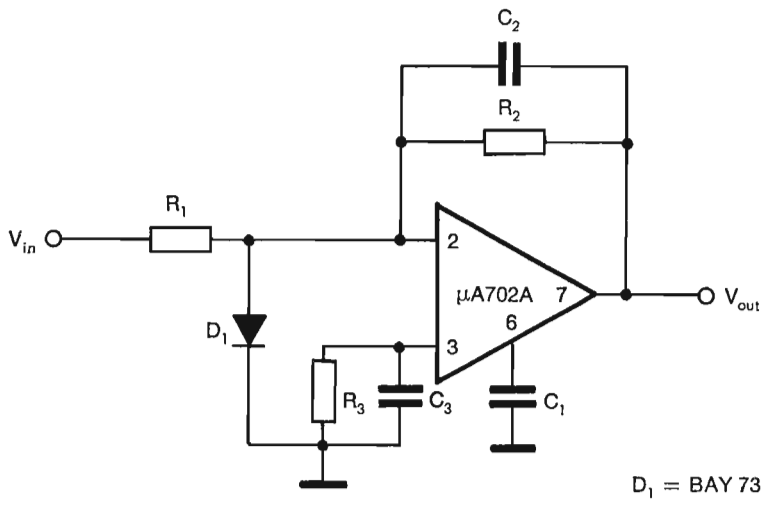


Fig. 3.11 - Low - Pass Amplifier

3.1.12 Band-Pass Amplifier

Fig. 3.12 shows the circuit for a simple selective amplifier using only one μA702A and a twin-T filter.

The ideal characteristics for the filter are such that where R_o is the output load resistance and R_{in} the source resistance then at a frequency f_o the attenuation is infinite and phase shift zero.

For optimum selectivity coupled with minimum phase shift in the region of f_o, then the values of the filter components are chosen such that:

$k' = 4\,k \qquad k = 0.5 \qquad R^2 = 2R_oR_{in}$

and the ratio $\frac{R_o}{R_{in}}$ should be as large as possible consistent with the remainder of the external circuitry.

The mid-point of the frequency response curve is given by:

$$f_o = \frac{1}{2\pi RC} \qquad \ldots\ldots (1)$$

At f_o the overall gain is given by:

$$A \approx \frac{R_2}{R_1}$$

Also the Q of the selective amplifier is defined as

$$Q \approx \frac{A_Q+1}{4}$$

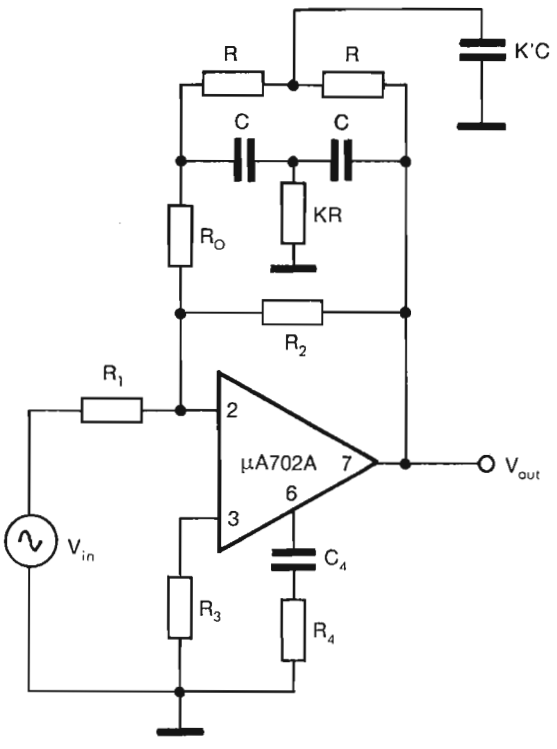


Fig. 3.12 - Band - Pass Amplifier

where A_Q is the gain of the loop into which the filter is inserted.

$$\text{Thus } A_Q \approx \frac{R_2}{R_o + \frac{R}{\sqrt{2}}}$$

Example of practical circuit:

Let $R = 910\,\Omega$ $\qquad f_o = 60$ KHz

$k^1 = 2$

$k = 0.5$

From Equation (1) we have

$$C = \frac{1}{2\pi R f_o} = 2930 \text{ pF}$$

Choosing $C = 3\,000$ pF which would give

$f_o = 57.8$ KHz and $R_o = 10\,k\Omega$ we have

$$R_{in} = \frac{R^2}{2R_o} = 41\,\Omega$$

The output impedance of the amplifier under closed-loop conditions will be in this order of magnitude so that chosing $R_o = 10\,k\Omega$ is reasonable.

If desired value for $Q = 10$ then:

$$A_Q \rightleftarrows 4\,Q - 1 = 39$$

$$\text{and } R_2 = (4\,Q - 1)\left(R_o + \frac{R}{\sqrt{2}}\right) = 415\,k\Omega$$

i.e., approximately $430\,k\Omega$.

If the overall gain is 100 then

$$R_1 = \frac{R_2}{A} = 4.3\,k\Omega$$

Typical bandwidth would be approximately 5.6 KHz between the -3 dB points. Maximum undistorted output is 2 V peak-to-peak.

Note (1). C_4 and R_4 are frequency stabilizing components and should have values of:

$R_4 = 43\,\Omega$

$C_4 = 2\,200$ pF

Note (2). R_3 should be approximately $4.3\,k\Omega$.

3.1.13 Band-Pass Active Filter

A very interesting application for integrated amplifiers is that of active filters using RC networks.

The limiting factor in filter design is often due to the use of heavy and cumbersome inductors. These may be replaced by suitable integrated amplifiers, thus saving valuable space.

Fig. 3.13 (a) shows a 4th order Butterworth band-pass filter having a relative band pass

$$B = \frac{\omega_1 - \omega_2}{2\omega_o} = 0.1$$

It is obtained by connecting two circuits, in cascade, each of which uses a μA702A integrated amplifier with a suitable RC network, and makes a quadratic function.

The total transfer function is:

$$F_{(p)} = \frac{2B\alpha RCs}{1 + 2\xi\alpha RCs + (\alpha RC)^2 s^2} \cdot \frac{\frac{2BRCs}{\alpha}}{1 + \frac{2\xi}{\alpha}RCs + \frac{RC^2}{\alpha}s^2} \quad \ldots\ldots\ldots (1)$$

where α RC = 1.073 and $\frac{RC}{\alpha} = 0.932$

$2\xi = 0.142$

Equation (1) is obtained through the conformal frequency transformation of the low-pass prototype transfer function.

The filter has been denormalized for a centre frequency of 10 KHz and making:

$$\frac{C}{\xi} = 20\,000 \text{ pF}$$

The filter using passive components at 0.5% has a bandwidth of 2 KHz at 3 dB and a centre attenuation (10 KHz) of 0.3 dB. Finally, Fig. 3.13 (b) and (c) show the filter frequency response measured experimentally.

Note: C_1 and R_1 provide frequency compensation.

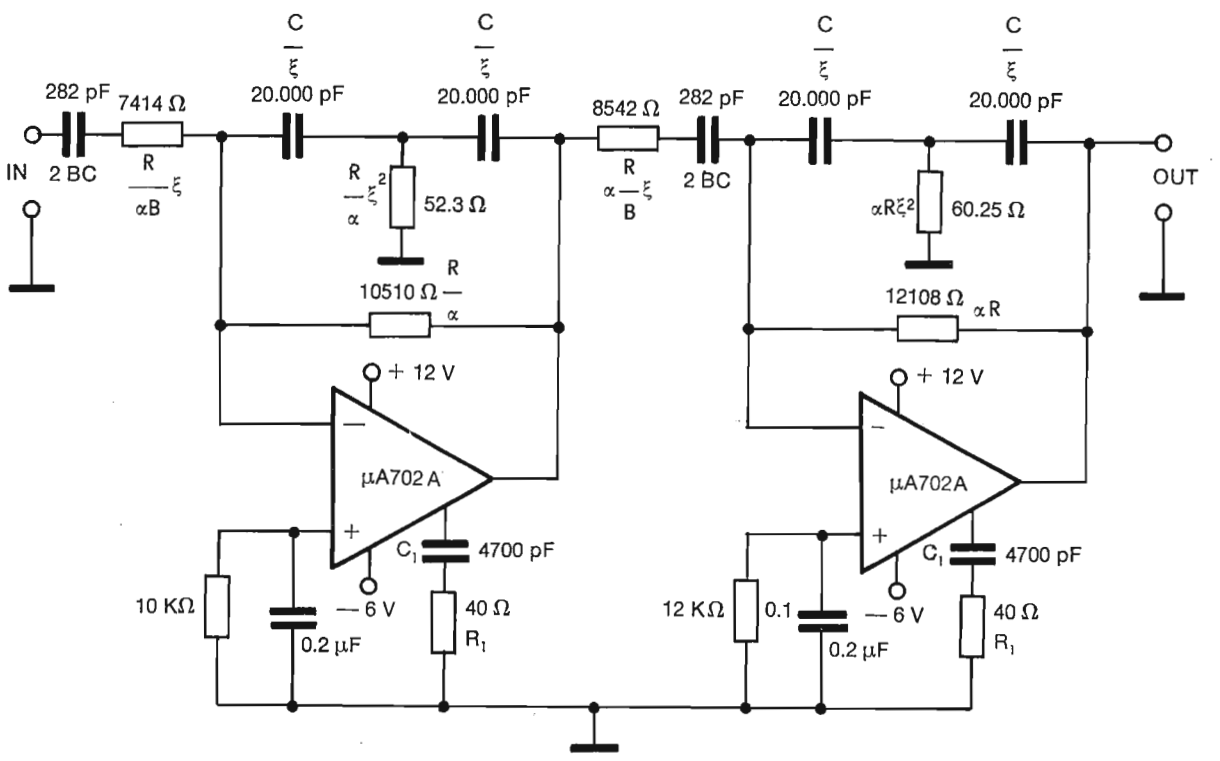


Fig. 3.13 (a) - Four Pole Butterworth Band-Pass Filter

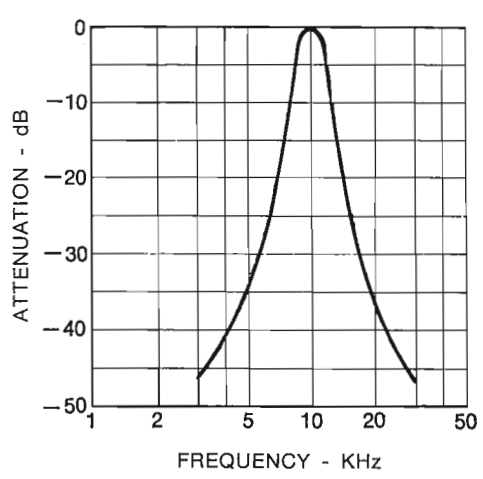


Fig. 3.13 (b) - Pass-Band Frequency Response At 10 KHz

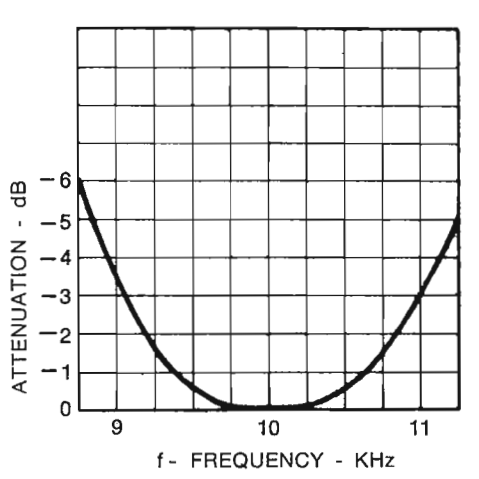


Fig. 3.13 (c) - Pass-Band Frequency Response at 10 KHz

A practical amplifier might have the values:

$R_1 = 51\ k\Omega$	$R_4 = 0$
$R_2 = 100\ k\Omega$	$C_1 = 4.7\ \mu F$
$R_3 = 51\ k\Omega$	$C_4 = 0.1\ \mu F$

This amplifier will have a voltage gain of approximately 3 and an input impedance > 5 MΩ. The L.F. 3 dB attenuation points is 1 Hz.

Note. For maximum bandwidth, the values of R_4 and C_4 may be optimised, see Frequency Compensation Section 5.

3.2.4 Solar-Cell Amplifier

Fig. 3.17 represents a circuit developed as a servo-amplifier in a system where light falling onto two solar cells is detected and amplified so as to drive a servo-positioning motor.

The polarity of the output depends on the relative strentgh of illumination between the two cells.

The common-mode operating point is at approximately — 3 V and the sensitivity 50 mV/μA. C_4 provides a conservative frequency response characteristic.

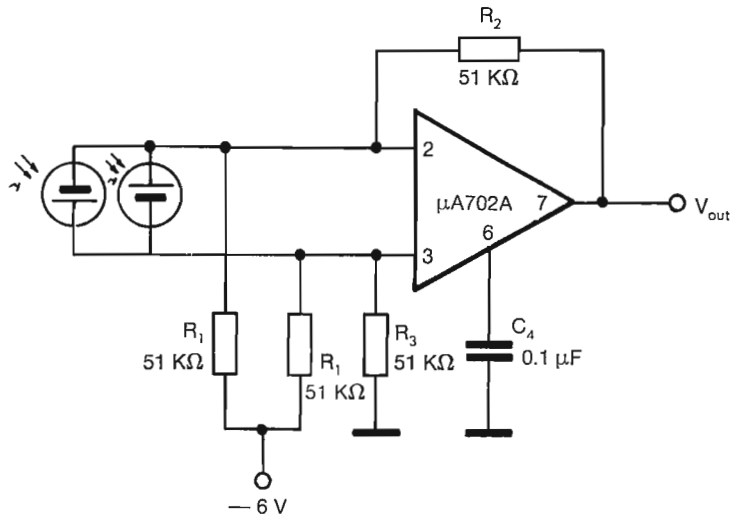


Fig. 3.17 - Solar Cell Amplifier

3.2.5 Tape-Head Video Amplifier

Fig. 3.18 shows a circuit with exceptionally large bandwidth suitable as preamplifier for a video tape pickup.

The extended bandwidth is obtained by lead compensation between pins (5) and (6) using $C_1 = 50$ pF. The voltage gain is given by the expression:

$$A_f = \frac{R_2 + R_1}{R_1} = 23 \qquad \ldots\ldots\ldots\ (1)$$

Since there is approximately 40 dB of feedback, it is necessary to provide additional frequency compensation (see Section 5). To avoid unduly limiting the output swing, this is best placed across the input terminals and consists of C_3 and R_3.

R_4 is the load resistance for the tape head. The bandwidth which is in excess of 15 MHz makes the amplifier sensitive to capacitance loading and this should be kept to a minimum and not exceed 50 pF without adjustment to the compensation networks resulting in loss of bandwidth.

By making the feedback resistor $R_2 = 11\ k\Omega$ the gain can be increased to approx. 220. In this case the bandwidth is reduced to 7 MHz. The frequency compensation network across the input terminals should no longer be necessary (see Section 5.2.3).

3.2.6 Photo-Diode Amplifier

Fig. 3.19 shows a circuit for a sensitive light level detector using a photo-diode.

With the photo-diode non-conducting the inverting input of the amplifier is returned to the positive supply via R_1. The negative output swing is limited to < — 1 V by the diode D_1 connected from pin (6), the lag frequency compensation point, and earth.

When the intensity of light causes the photo-diode current to exceed approximately 4 μA, the voltage at pin (2) commences to go negative with respect to that at pin (3).

The output voltage and positive feedback via R_5, R_6 and R_4 to the base of TR_2 causes the output to be driven into saturation at approximately 10 V positive.

TR_1 and TR_2 is a dual, low-noise and matched high gain (at low current) device, used in an emitter-follower configuration to increase the input impedance to the μA702A.

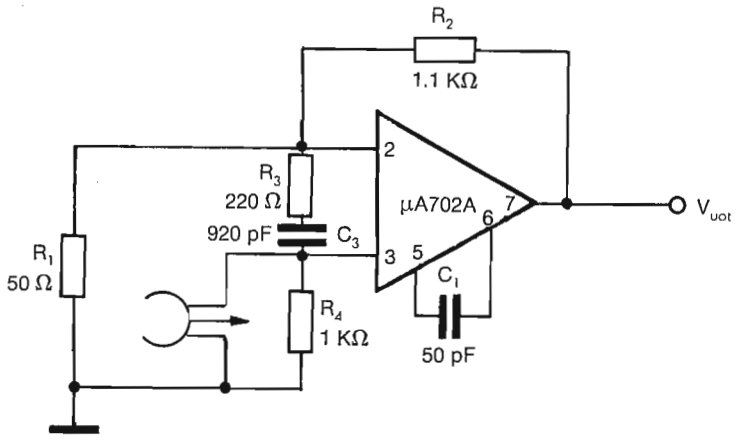


Fig. 3.18 - Tape Head Video Amplifier

The hysteresis voltage is given by:

$$V_h = \frac{R_6}{R_5+R_6}\,(V_{out(max)} - V_{out(min)}) \quad \ldots\ldots\ldots\ldots (1)$$

With the values shown:

$$V_h = \frac{2}{2+220}\,(V_{out(max)} - V_{out(min)})$$

and assuming that $(V_{out(max)} - V_{out(min)}) \approx 11$ V

$$\therefore V_h \approx \frac{2(11)}{222} \approx 0.1 \text{ V}$$

This gives a photo-diode hysteresis current ($i_{d(h)}$)

$$i_{d(h)} = \frac{V_h}{R_1} \approx \frac{0.1}{3\text{x}10^{-6}} \approx 0.03\ \mu\text{A}$$

Note (1). Should this circuit be used for driving logic then Section 2.4.3 should be consulted.

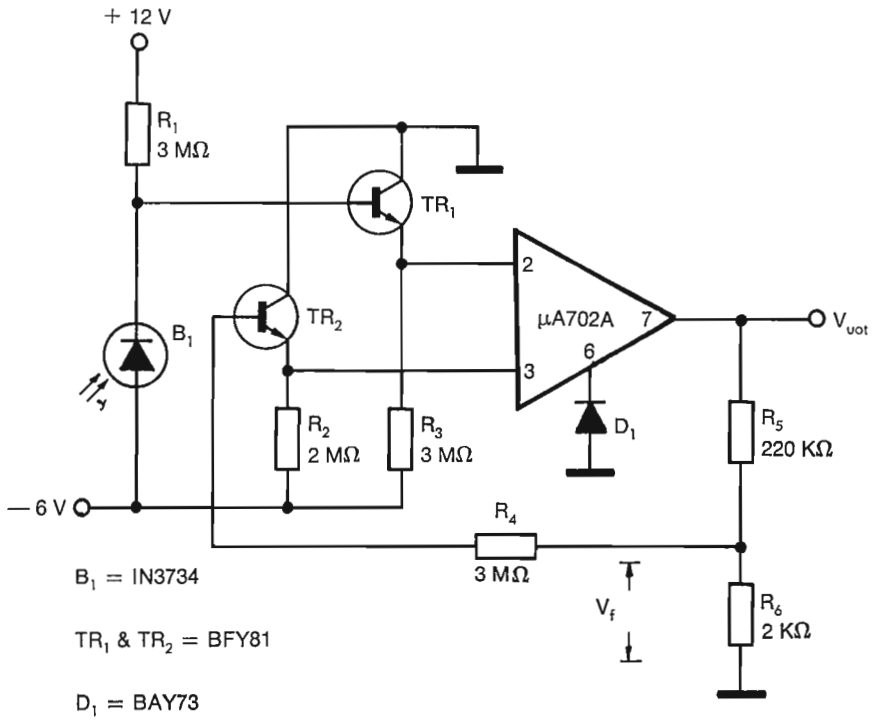


Fig. 3.19 - Photodiode Amplifier

3.2.7 Half-Wave Rectifier

For conventional diode rectification or detection circuits, the voltage drop across the PN junction when conducting in the forward direction may give rise to considerable errors (i.e., distortion, loss of rectification efficiency, etc.), particularly in low-level signal applications. Fig. 3.20 shows a circuit which effectively overcomes these disadvantages in a half-wave rectifier configuration.

For a positive input, the output is zero with an output impedance of 10 kΩ.

For a negative input, the output is given by

$$V_{out} \approx -V_{in}\frac{R_2}{R_1} \qquad \text{..... (1)}$$

It can be seen that the forward voltage drop across D_3 (typically 0.7 V) is effectively divided by the open-loop gain of the μA702A and is therefore less than 1 mV.

By a suitable choice of values for R_2 and R_1, the circuit will, in addition, provide amplification.

Note (1). C_4 and R_4 provide frequency compensation.
Note (2). D_2 protects against possible latch-up and excessive positive input transients.

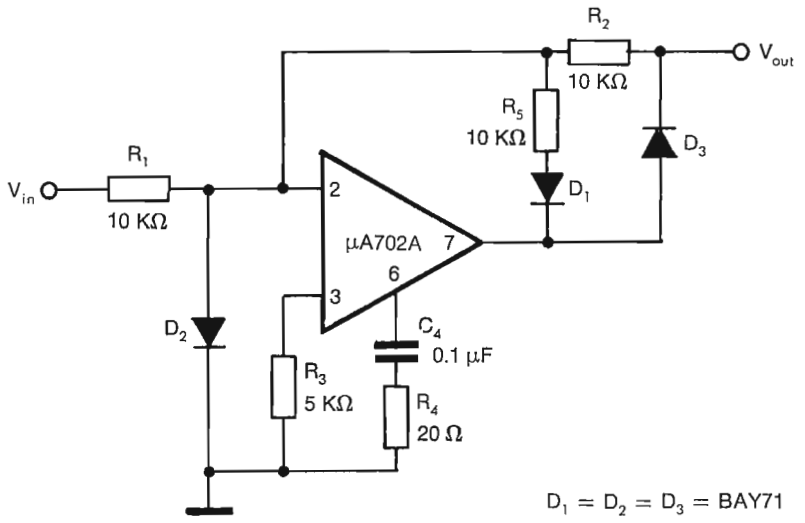


Fig. 3.20 - Half-wave Rectifier

3.2.8 Peak Detector

The half-wave rectifier circuit of Fig. 3.20 may be modified to act as a peak voltage detector by the addition of C_1, see Fig. 3.21.

The output is zero for positive input and V_{out} attains the peak positive voltage equivalent to the peak negative input signal.

The method of operation is that as V_{in} goes negative the voltage at pin (7) goes positive (amplified by the open-loop gain) charging C_1 via R_6 and D_1 until equilibrium is reached:

$$\text{i.e., } \frac{V_{out}}{V_{in}} = \frac{-R_5}{R_1} \qquad \text{..... (1)}$$

The decay time for this output voltage is obtained from the time-constant:

$$C_1 \cdot \frac{R_5 R_L}{R_5 + R_L} \qquad \text{..... (2)}$$

where R_L is the load resistance.

The response time of the circuit may be approximately estimated by considering the charge path of C_1. This consists of $R_o + R_6 + R_d$ where

R_o = Open-loop output impedance of amplifier (≈200 Ω)

R_d = Forward impedance of D_1 (≈50 Ω)

R_6 = Output current limiting resistor (100 Ω)

Assuming the open-loop gain is approximately 2 000 then where $|V_{out}| \sim |V_{in}| > 5$ mV then amplifier is saturated and μA702A output is > +10 V.

C_1 may be considered to be charging from a 10 V source through approximately 350 Ω for this condition. The charging circuit for the last 5 mV requires more detailed analysis and, for most applications, probably produces negligible error.

Note (1). D_2 protects against possible latch-up or excessive input voltage.

Note (2). R_3 provides temperature stability and minimum offset where $R_3 \approx \frac{R_1 R_5}{R_1 + R_5}$

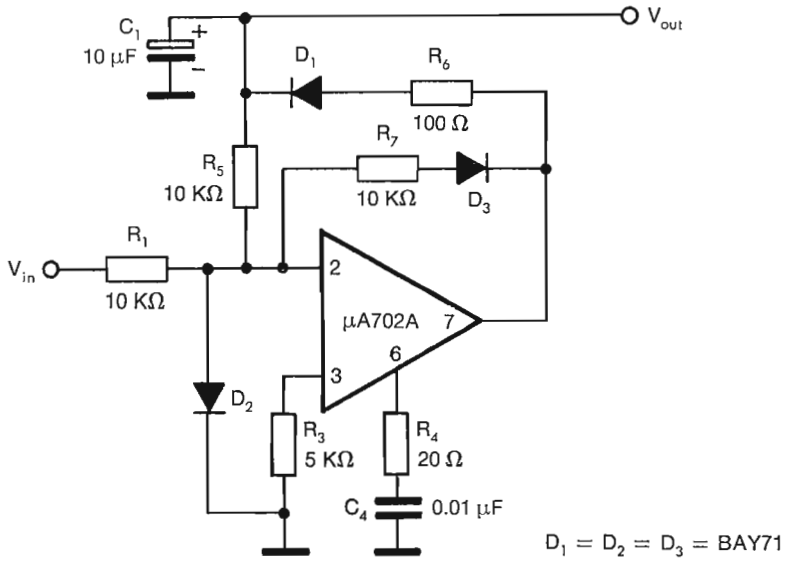


Fig. 3.21 - Peak Voltage Detector

Note (3). D_3 and R_7 are a refinement which ensures that pin (2) always act a « virtual earth » point. Also by keeping the amplifier loop gain at unity for positive inputs, hard negative saturation does not occur which improves the response to short-duration input pulses.

Note (4). R_4 and C_4 provide frequency compensation

3.2.9 Full-Wave Rectifier

Fig. 3.22 shows a circuit of an absolute value or full-wave rectification circuit where the normal forward voltage drop V_f of the diode is almost eliminated.

The first µA702A acts as a unity-gain, half-wave rectifier giving negative output for positive input signals.

This output is fed, together with the original signal, into pin (2) of the second µA702A acting as a summing amplifier via R_6 and R_{10} respectively. Because of the ratios $\frac{R_8}{R_{10}}$ and $\frac{R_8}{R_6}$ the second amplifier ope-

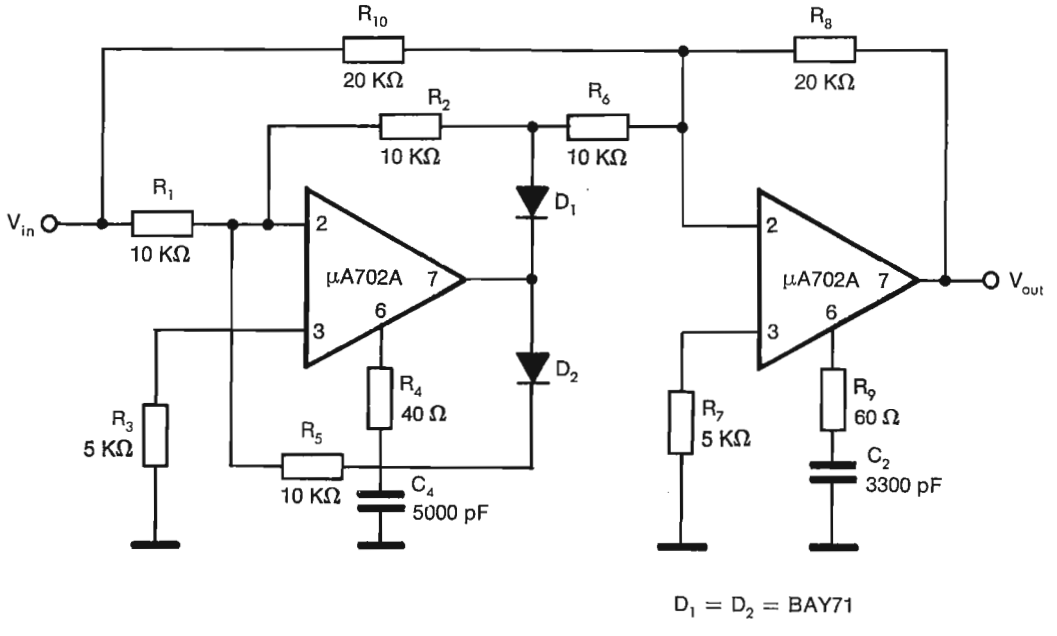


Fig. 3.22 - Full Wave Rectifier

rates with unity gain to the original signal and x2 for the half-wave output signal.

The net effect is that the output is always positive-going and gives the absolute value of the input since for negative V_{in} the input is directly into the summing amplifier via R_{10} while the half-wave output is zero. For positive inputs, the addition of the signals via R_{10} and R_6 gives a net negative input equivalent to unity-gain positive output.

Note (1). R_3 and R_7 provide thermal stability and minimise offset voltage.
Note (2). R_4 C_4 and R_9 C_2 are for frequency compensation.

3.2.10 Current Source Generators
(a) Grounded Load Current Generator

Fig. 3.23 (a) shows a suitable circuit for a current generator to a load having one end earthed. It may

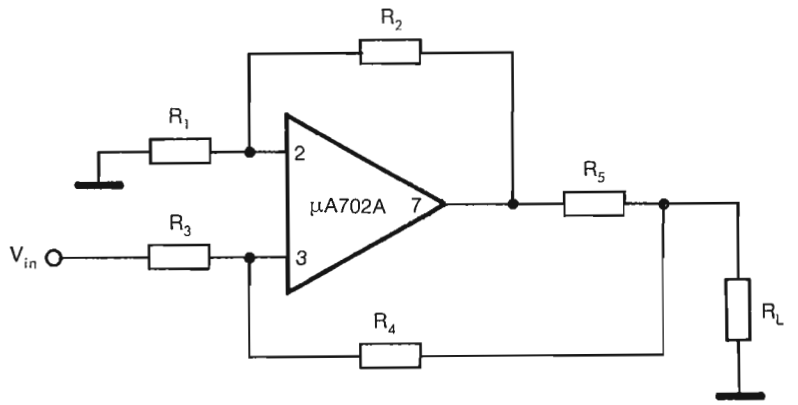


Fig. 3.23 (a) - Current Source Generator Grounded Load - Basic Circuit

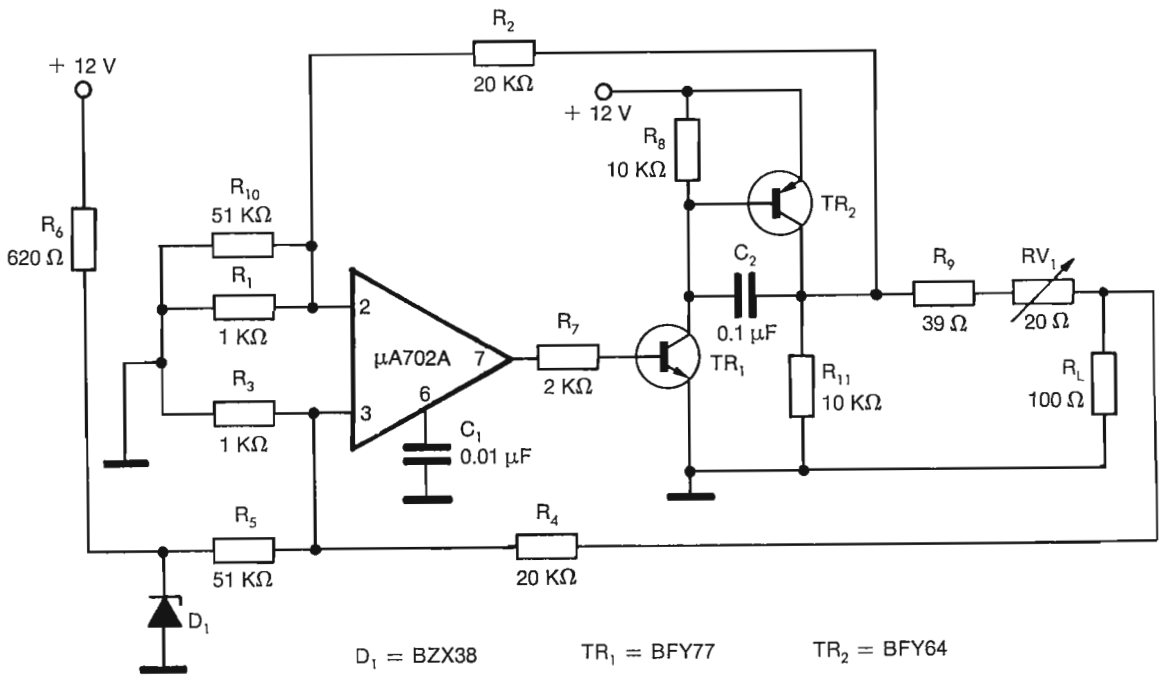


Fig. 3.23 (b) - Grounded Load — Practical Circuit

be shown that, if R_2 and $R_4 \gg R_L$ so that the currents flowing through R_2 and R_4 are negligible compared with i_L, then an expression for the load current may be given by:

$$i_L = V_{in} \frac{R_4}{R_3} \cdot \frac{1}{R_5} \qquad \text{..... (1)}$$

Where $\frac{R_2}{R_1} = \frac{R_4}{R_3}$

It should be noted that care has to be taken to avoid exceeding the common-mode operating voltage limit above +0.5 V by limiting the voltage developed across R_L such that:

$$(V_L + i_L R_5) \frac{R_1}{R_1 + R_2} < 0.5\ \text{V} \qquad \text{..... (2)}$$

Fig. 3.23 (b) shows a practical crcuit where V_{in} is constant and the current level is set by adjustment of RV_1. The values indicated are suitable to provide a load of 100 Ω with a current of 50 mA.

(b) **Floating Load Current Generator**

Fig. 3.23 (c) shows the basic circuit of a current generator where the load is floating, i.e., neither side is grounded. The expression for the load current i_C, assuming infinite open-gain for the amplifier, is as follows:

$$i_C = V_{in} \cdot \frac{R_2}{R_1} \cdot \frac{1}{R_4} \qquad \text{..... (3)}$$

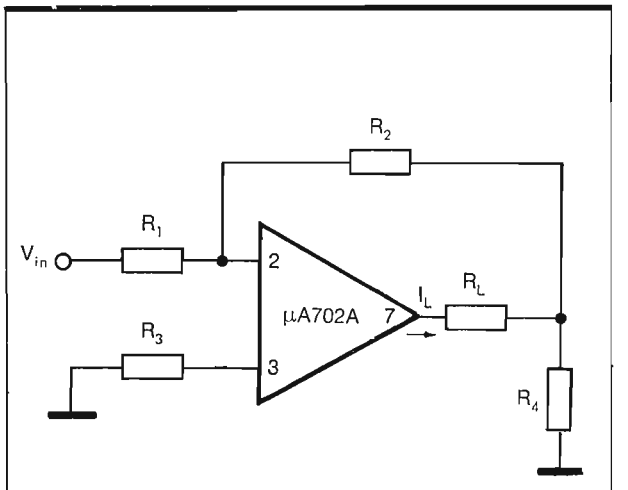


Fig. 3.23 (c) - Floating Load — Basic Circuit

Fig. 3.23 (d) shows a practical example of a circuit capable of delivering currents up to 50 mA depending on the load resistance and with suitable values of R_1 and R_2.

V_{in} is kept constant and is provided by the Zener diode Z_1 (6.8 V). The current level is adjusted by means of RV_1 and, for the values shown, would give a current of approximately 35 mA at mid-point. C_1 and C_2 are for stability purposes.

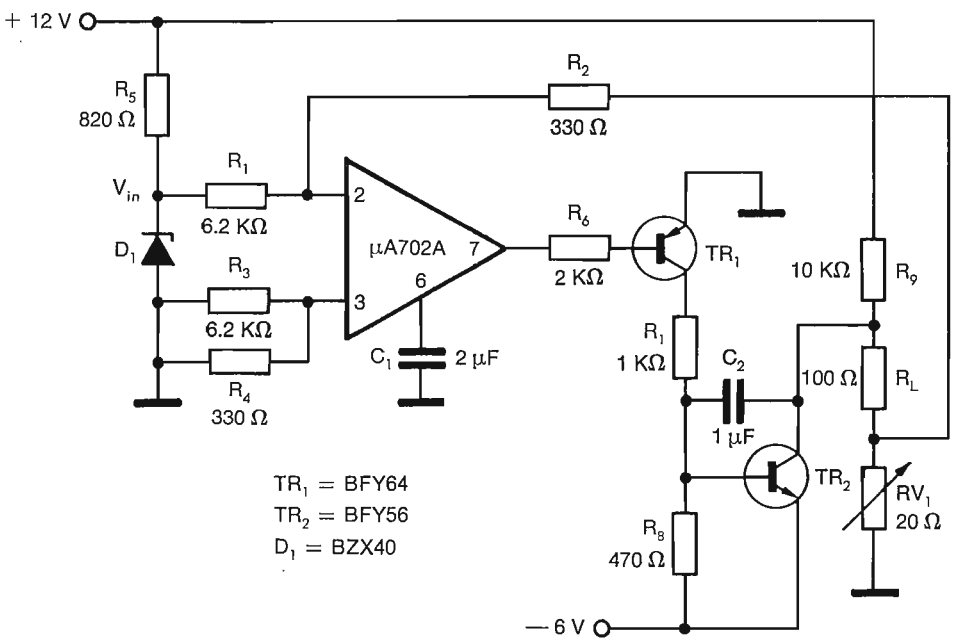


Fig. 3.23 (d) - Floating Load — Practical Circuit

3.2.11 Sine-Wave Oscillator

Fig. 3.24 shows the circuit diagram of a phase-shift-oscillator. Negative feedback is applied to the inverting input of the amplifier through R_3 to stabilize the gain and make it essentially independent of the integrated circuit characteristics. The RC network (C_1, R_1, R_2, and C_2) applies positive feedback to the non-inverting input. The circuit will oscillate at the frequency where the phase shift through the RC network is zero, as long as the positive feedback is equal to or greater than the negative feedback. It is desirable to maintain the positive feedback exactly equal to the negative feedback: if the positive feedback is greater, the output of the oscillator will build up until it becomes non-linear, thereby distorting the output sine wave. The positive and negative feedback cannot be made equal with a simple adjustment since any small component change will either cause the circuit to stop oscillating or distort. This difficulty is overcome using an AGC circuit which holds the gain at the precise value required to sustain oscillation at the desired output level.

If $R_1C_1 = R_2C_2$, the frequency where the phase shift through the RC network is zero (and therefore the frequency of oscillation) is given by

$$f = \frac{1}{2\pi R_1 C_1} \qquad \text{..... (1)}$$

The attenuation through the network at this frequency is

$$\eta = \frac{1}{1 + \frac{2R_1}{R_2}} \qquad \text{..... (2)}$$

The amplifier gain must make up for this loss for oscillation to be possible. For $R_1 = 10R_2$ the amplifier gain must be exactly 21. A large ratio of R_1 to R_2 is chosen to keep the signal level across the gain-regulating FET enough to avoid distortion.

The output of the amplifier is rectified by D_1 and filtered by C_4. This voltage, which varies as the A.C. output of the amplifier, is fed to the gate of the FET. The drain-to-source resistance of the FET is controlled by this voltage to hold the output of the amplifier at a constant level. The filter capacitor, C_4, must be large enough for stability of the AGC loop. The value of C_3 is also important for AGC stability. To change the frequency of oscillation, C_1, C_2, C_3, and C_4 should all be changed in proportion. The A.C. output level is determined by the ratio R_6/R_5 and the characteristics of the FET.

With the component values shown, the frequency of oscillation is 1 KHz and the peak-to-peak output voltage is about 8 V. The stabilization time from initial turn-on is approximately 50 milliseconds.

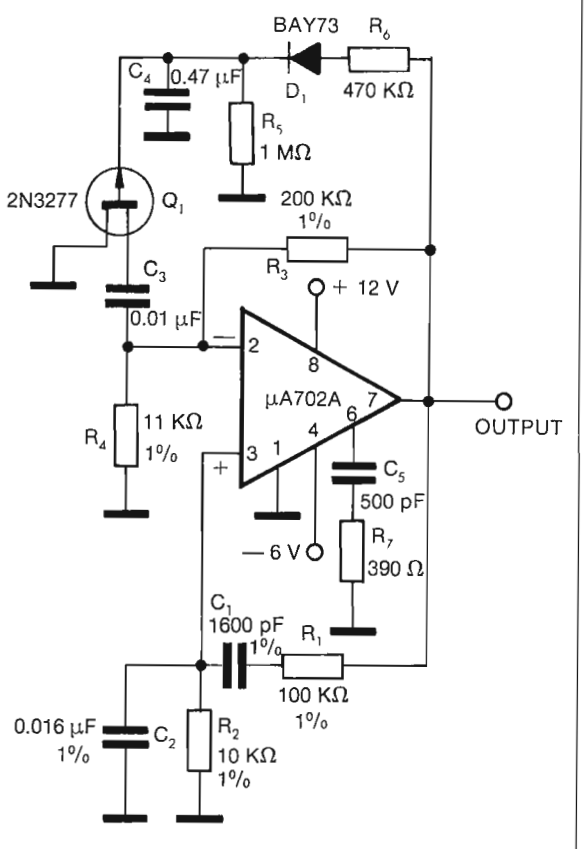


Fig. 3.24 - 1 KHz sine-wave Oscillator

3.2.12 Zero-Crossing Detector

Often in the processing of electrical analogue data, a power spectrum analysis of some particular signal waveform must be performed. This procedure requires that the frequency content of the signal waveform of interest, within a specified passband, be extracted from the broadband signal and noise. A zero-crossing detector using the µA702 operational amplifier provides a simple and effective means of performing such an operation.

A zero-crossing detector is a device which changes state each time the analogue input signal passes through zero (or through its average reference level). The input signal is thus converted into a train of frequency-dependent pulse-widths. The resultant zero-crossing intervals then may be examined for frequency content.

This « infinite » clipping of the signal virtually eliminates distortion caused by amplitude fluctuations, circuit variations, and noise, and permits simplification of further data processing though the use of digital techniques. These features are especially valuable for information processing systems where

signal storage and correlation processes are to be utilised, such as in digital beamformers and correlators.

The commonly used Schmitt trigger and multistage limiter-clipping circuits can exhibit large errors in zero-crossing information. The Schmitt trigger introduces distortion due to its large « on-off » hysteresis characteristic. The circuit does not change state when the input signal passes through zero, but at different levels for positive-going or negative-going signals.

Distortion in multistage limiters is caused by a shift in the average reference level after each successive stage of limiting. The shift in average level arises because the signal cannot be fully clipped in one operation. Large peaks (which may be of one polarity only) are clipped by the first stages of the limiter, thus altering the waveform to produce a different average level. The following limiter stage then clips the resultant signal about the new average level, which can completely change the character of the original signal.

The large voltage gain and dynamic range of the μA702A permit full clipping of a signal by a single stage of processing. The circuit shown in Fig. 3.25 exhibits a nearly ideal transfer characteristic for a zero-crossing detector.

The amplifier has full open-loop gain (about 70 dB) when the output is less than the forward voltage limits of the diode network, and it has very little gain outside this range. Thus, an extremely wide dynamic range of input signals, including small voltage excursions of the order of ± 500 microvolts, will completely drive the amplifier to the maximum output of ± 1.5 volts. A random analogue waveform fed into the input of the circuit thus will be uniformly clipped with negligible hysteresis or loss of average reference level.

A useful variation of the basic circuit is obtained by replacing R_1 in Fig. 3.25 by a capacitor. The output signal then changes state each time the input signal passes through an amplitude peak rather than through zero. Since the signal rate of change is zero at an amplitude peak, this peak-detector circuit functions as a zero-crossing detector for the first derivative of the input signal.

The use of both zero-crossing detectors and peak-detectors results in simple, accurate data processing systems. For example, a position pick-off

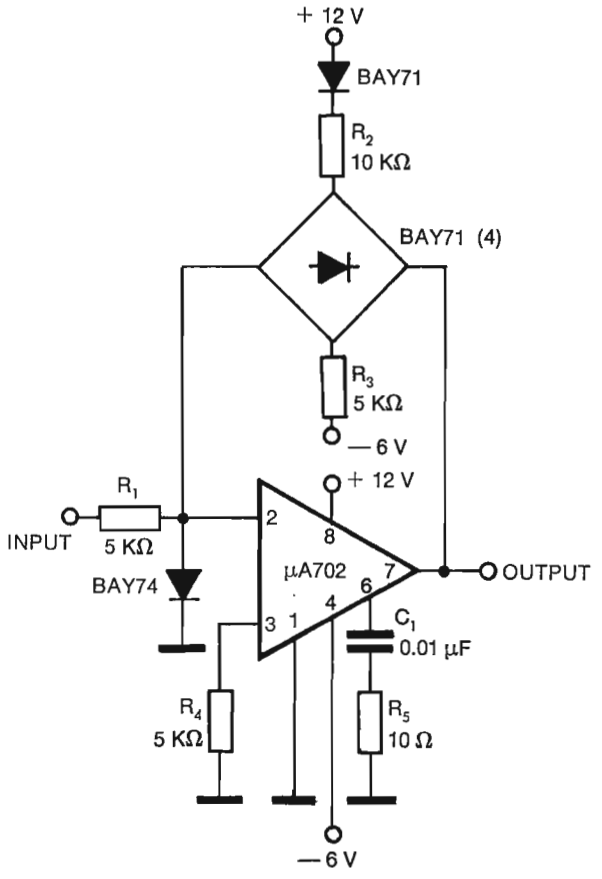


Fig. 3.25 - Zero-Crossing Detector

sensor, monitored by both circuits, would provide precise information regarding the time at which the system being measured passed through its rest position (x = 0) and when its velocity reached zero

$$\left(\frac{dx}{dt} = 0 \right)$$

These signals may be used as final output information, or may serve as timing or gating signals to initiate synchronous sampling of other instantaneous functions. The simplicity, reliability, and extremely small size of the μA702 permit many such circuits to perform complex data processing in any easy and convenient manner.

3.2.13 Power Supply

Fig. 3.26 shows a stabilized power supply with an output voltage range variable from 1 V to 24 V, and able to deliver a current of 100 mA where the μA702A acts as an error amplifier.

The μA702A is separately supplied by the series-connected regulating transistor in such a way that the output voltage and current delivered from the power supply are defined by the power which can be dissipated, and by the breakdown voltage of the actual transistor.

The output transistor is provided with a proper heat-sink in order to allow for a permanent short-circuit up to an ambient temperature of 50°C.

Within the dotted area of the circuit diagram is the output current-limiting circuit.

The output current of TR_2 causes a voltage drop across $R_7 + P_2$ which, when it reaches the threshold voltage of TR_3 causes it to conduct. Consequently the current of the μA702A output transistor and the regulating transistor decreases.

In fact, as the output voltage decreases the current remains constant; in this region the power supply can be considered as current generator with an output impedance of about 30 kΩ.

The maximum current delivered can be easily adjusted in the range between 10 mA and 100 mA by means of potentiometer P_2.

The capacitor C_1 at the output is used to reduce ripple and noise to about 2 mV and to ensure, in conjunction with capacitor C_2, the necessary stability with frequency response of the whole system.

The output voltage is stabilized to within ± 10 mV for input voltage variations of ± 20%, and for load currents between 0 to 100 mA; it can be altered from 1 V to 24 V by adjusting potentiometer P_1.

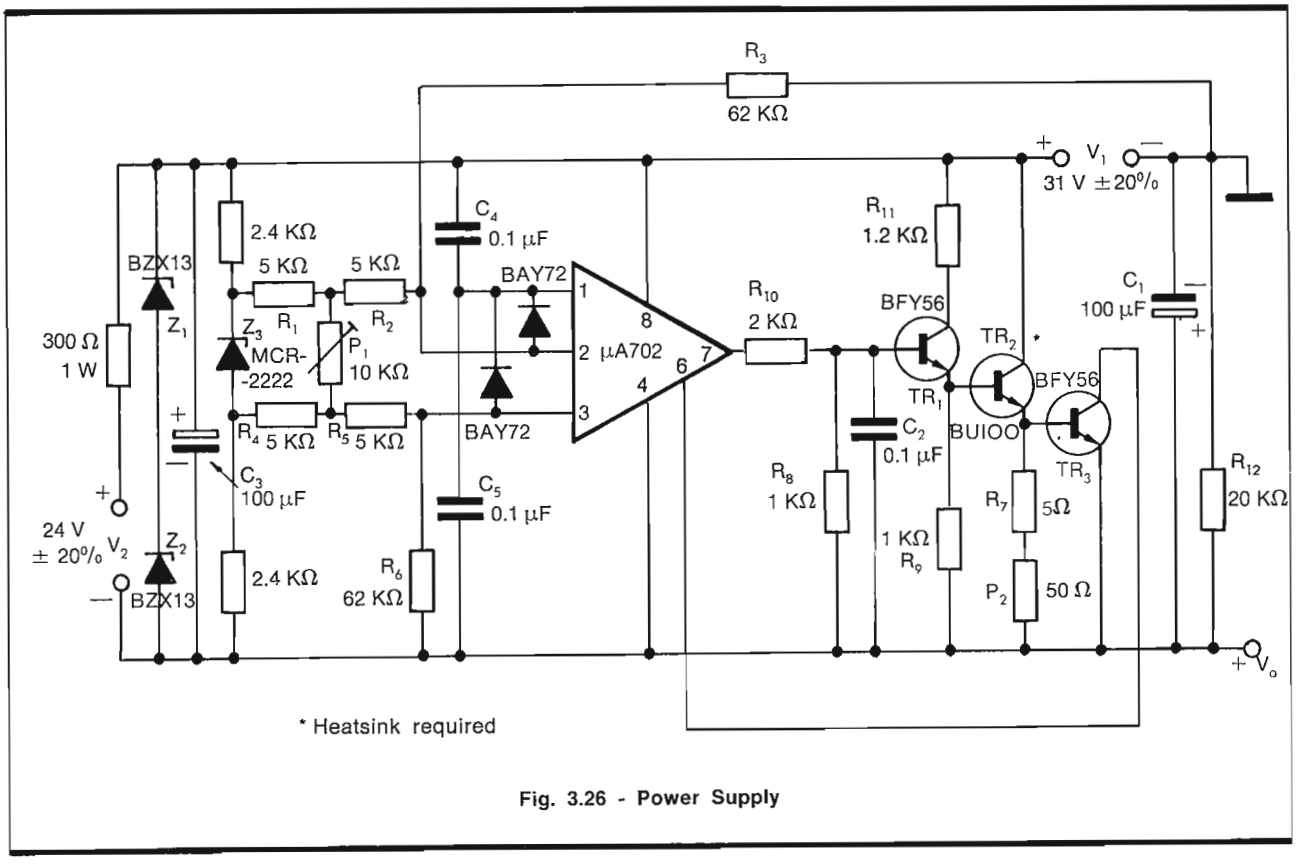


Fig. 3.26 - Power Supply

3.2.14 Servo Current Driver

Fig. 3.27 shows a push-pull, Class-B, servo current driver.

The output current of opposite sides is sensed across R_8 and R_{13}. One μA702A (A_1) functions as a unity-gain, non-inverting amplifier that makes the voltage across R_8 equal to the input voltage for positive input signals. For negative input signals, A_2 functions as a unity-gain, inverting amplifier that forces the voltage across R_{13} to be equal to the input voltage. Thus, phase inversion for the push-pull amplifier is obtained. The quiescent output current of the amplifier is determined by R_4 and R_9. The values shown give a quiescent current of approximately 20 mA on each side. The circuit will give a ± 2 A output current for a ± 2 V input signal. The input resistance is 4 kΩ.

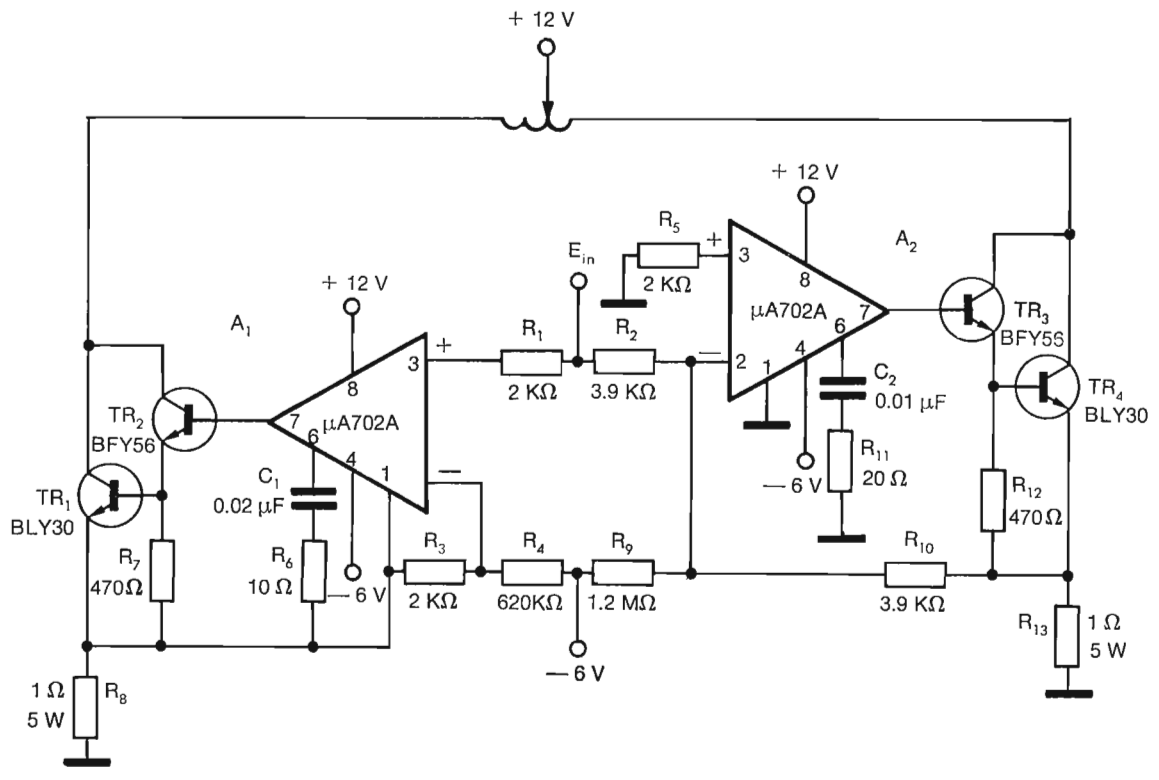


Fig. 3.27 - Class-B Servo Current driver

It is immediately obvious that the excellent D.C. characteristics of the μA702A permit biasing of the output stage at very low quiescent currents without running the risk of thermal runaway or of encountering a dead zone — even for operation over the full temperature range. It is also apparent that the low offset and high gain allow good accuracy without wasting an excessive amount of the supply voltage across the current-sensing resistors. Since the output transistors are included within the feedback loop, their characteristics have a negligible effect overall performance.

One unusual aspect of this circuit is that the ground terminal of A_1 (pin 1) is connected to the current-sensing resistor, R_8. This provides bootstrapping on the common-mode range of the amplifier so that it can be operated above its usual common-mode limit of + 0.5 V without exceeding ratings.

3.2.15 Voltage-to-Frequency Converter (a)

Fig. 3.28 (a) shows a circuit which may be used as a voltage analogue-to-frequency converter.

The μA702A in conjuction with TR_1 acts as a precision constant-current generator proportional to the input voltage to the non-inverting terminal (pin 3).

TR_2, C_2 and T_1 act as a blocking oscillator circuit with a repetition frequency which is directly proportional to the rate of charge of C_2 to a critical voltage V_t at which TR_2 commences to conduct.

The expression for the transconductance of the current generator is:

$$g_m = \frac{(R_2+R_1)}{R_1} \cdot \frac{1}{(R_6+RV_2)} \cdot \frac{h_{FE}}{(h_{FE}+1)} \quad \ldots . (1)$$

where h_{FE} is the D.C. current gain of TR_1.

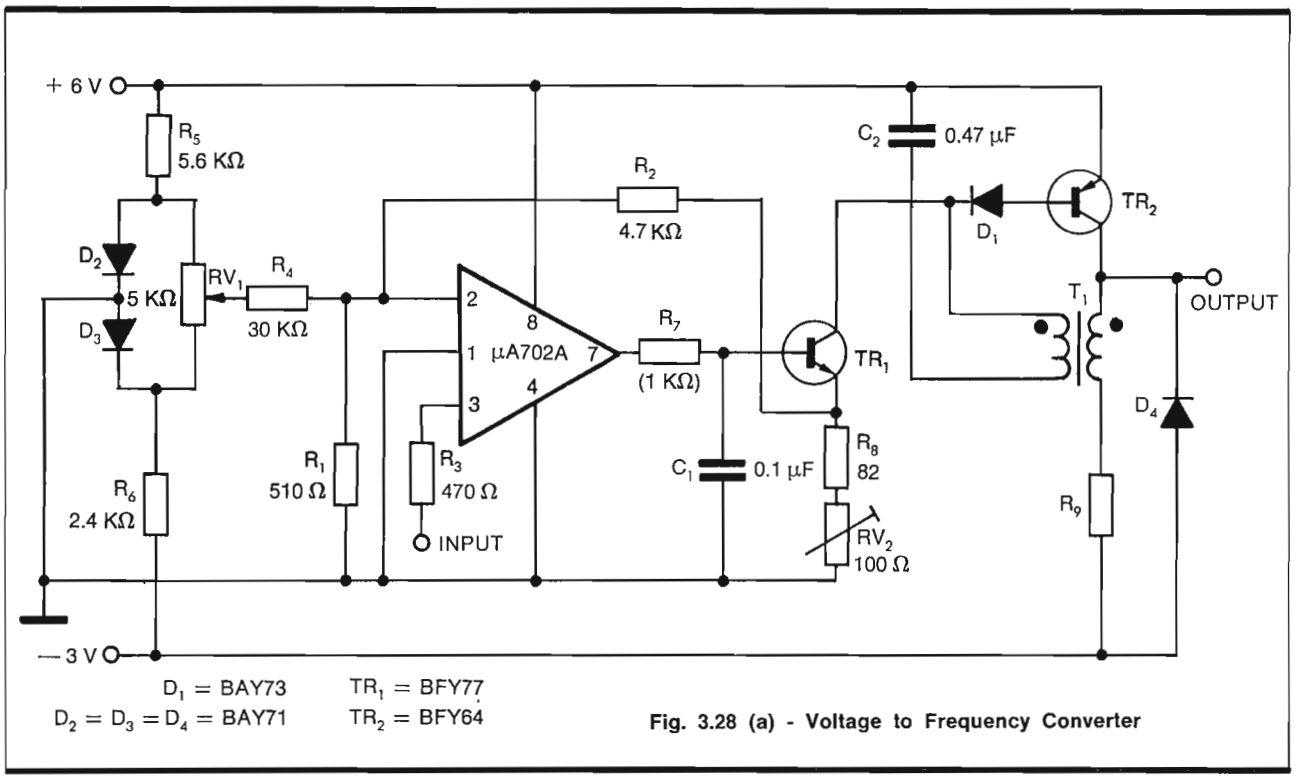


Fig. 3.28 (a) - Voltage to Frequency Converter

Since TR_1 is chosen to have very high h_{FE} down to low current levels (typically 290 at 100 μA), the g_m is determined almost entirely by resistor ratios.

D_1 is a low-leakage current diode in series with the base of TR_2 to reduce the normal I_{EBO} which would tend to cause non-linearity at very low charging currents. C_2 should be a low-loss non-polarised capacitor such as the « Mylar » type.

Note (1). C_1 R_7 provide frequency compensation and reduce noise voltage. R_7 also prevents the possibility of excessive current being delivered from the output of the μA702A.

Note (2). D_4 provides a reset current path for the blocking oscillator transformer.

Note (3). R_9 limits the maximum current through TR_2 to a safe level.

Note (4). The transformer T_1 consisted of 20 turns of 0.16 mm diameter wire for both the primary and secondary. The core was a Philips toroidal type K300437/3HI.

The amplitude of the output pulse should be approximately the difference between the supply rails (i.e. + 9 V) and the duration is dependent on the volt-second storage capacity of the transformer core. The pulse duration should, in any case, be made very much smaller than the maximum repetition rate expected from the oscillator.

This circuit was originally developed for a thermocouple input signal where the offset voltage compensating potentiometer RV_1 was adjusted to give an output frequency of ≪0.5 Hz for zero input voltage and V/f scaling was carried out by means of RV_2 to give 200 pulse/sec. for a 5 mV input.

The overall performance of the circuit is dependent on the stability of the power supplies and enviromental temperature but for a given set of conditions, linearity better than 0.5% can be expected.

Voltage-to-frequency converter (b)

Fig. 3.28 (b) shows a voltage-to-frequency converter consisting of an integrator, a voltage comparator and switch. The output voltage of the integrator is a negative-going ramp which falls at a rate that is directly proportional to the D.C. input signal. When the output of the integrator reaches a predetermined negative level, it is sensed by the comparator which drives the switch to reset the integrator output to zero; the cycle is then repeated. The time required for the integrator output to go from zero to the preset level is inversely proportional to the input voltage so the operating frequency will be proportional to this voltage.

The μA702A is chosen for the integrator because of the fast slewing rate required during the reset interval. However, the μA702A alone does not have enough gain to make the integrator function properly over a wide dynamic range. In addition, lower input currents than are practical with the μA702A are frequently required in this application. Both these limitations are overcome by using a discrete PNP matched pair (TR_1 and TR_2) in front of the amplifier. This composite amplifier has a gain greater than 25 000 and input currents less than 0.5 μA. The offset voltage of the input transistors is conveniently balanced out with the potentiometer (R_6) shown in the circuit. Because of the high gain of the complete

amplifier, frequency compensation is done at two points with R_7 - C_1 and R_8 - C_3 as shown in the figure.

The integrating capacitor is C_4. The clamping diodes (D_1 and D_2) prevent overloading of the comparator under abnormal operating conditions.

A second μA702A is used as a voltage comparator at the output of the integrator. A threshold voltage of —4 V is supplied to the non-inverting input of the comparator from a resistive divider (R_{10} and R_{11}). When the output of the integrator falls to —4 V, the output of the comparator rises rapidly from —5 V, turning on TR_3 which supplies positive feedback to the non-inverting input of the comparator. TR_3 saturates and drives approximately 11 mA into the summing node of the integrator; it also holds the non-inverting input of the comparator very near to ground potential. When the integrator output, which is being driven positive by the switch current, reaches zero, the comparator output swings negative and turns off TR_3. The cycle is then repeated. In Fig. 3.28 (b) R_{12} limits the base drive of TR_3 while C_5 and C_6 decrease the turn-on and turn-off times of the switch.

The time required for a given change in the output voltage of the integrator is given in terms of the input voltage and circuit values by

$$t = R_1 C_4 \frac{\Delta E_{OUT}}{E_{IN}} \qquad \ldots\ldots\ (1)$$

Similarly, when TR_3 is turned on, the reset time is

$$t_r = C_4 \frac{\Delta E_{OUT}}{I_{C3}} \qquad \ldots\ldots\ (2)$$

or

$$t_r \cong R_{11} C_4 \frac{\Delta E_{OUT}}{V^-} \qquad \ldots\ldots\ (3)$$

The output of the integrator swings from zero to a voltage determined by the resistive divider, R_{10} and R_{11}, so

$$\Delta E_{OUT} = \frac{R_{10} V^-}{R_{10} + R_{11}} \qquad \ldots\ldots\ (4)$$

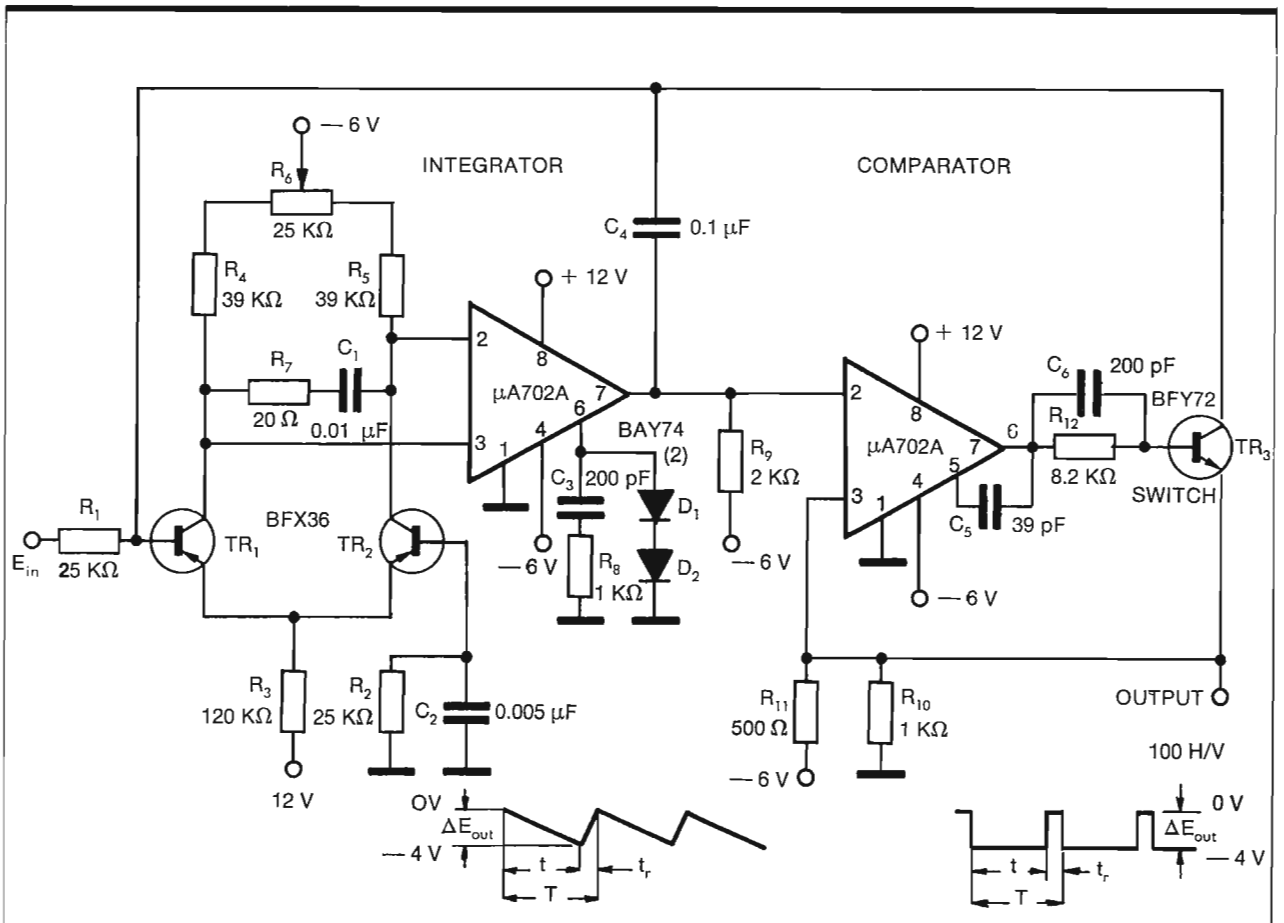


Fig. 3.28 (b) - Voltage-to-frequency Converter

Therefore, the period for one cycle of operation is

$$T = \frac{C_4 R_{10} V^-}{R_{10}+R_{11}} \left(\frac{R_1}{E_{IN}} + \frac{R_{11}}{V^-} \right) \quad \ldots (5)$$

Since $\frac{R_1}{E_{IN}} \gg \frac{R_{11}}{V^-}$, we can write

$$f \cong \frac{(R_{10}+R_{11})\, E_{IN}}{C_4 R_1 R_{10} V^-} \quad \ldots\ldots\ldots\ldots (6)$$

This gives a conversion factor of 100 Hz/V.

3.2.16 Transformerless Phase Detector

Fig. 3.29 shows a circuit developed as a 400 Hz transformerless phase detector. The first μA702A is used without feedback to produce switching pulses to TR_1 base. The network R_1C_2 is used to produce a phase lag of 90° with respect to the input reference signal $V_{(Ref)}$.

The second μA702A acts as a differential amplifier into which $V_{(Ref)}$ and $V_{(in)}$ are fed. The output voltage from pin (7) will, in general, swing about zero potential. The output V_o is the integral of the voltage present at pin (7) during the period of each cycle for which TR_1 is switched on.

Even when $V_{(in)}$ and $V_{(Ref)}$ are in phase, they will not necessarily be of the same amplitude. The difference in amplitude will result in a sine-wave output at pin (7). Since, however, the switching pulse has been displaced in phase by — 90°, then the output integrates to zero, having swung symmetrically about zero during the « on » period.

If $V_{(in)}$ is not in phase with $V_{(Ref)}$, then the output at pin (7) will not be symmetrical about zero for the « on » period and there will be a resultant output V_{out} which will be negative if V_{in} leads on $V_{(Ref)}$, and positive if it lags.

Note (1). When pin (7) is negative, TR_1 acts as an emitter-follower with R_9 as the emitter load. Where pin (7) is positive, then the emitter and collector are reversed in role such that R_9 becomes the collector load. There is, however, adequate base current drive to saturate the switch in this configuration though there is some loss in output voltage symmetry.

Note (2). D_1 blocks the positive-going output from the first μA702A and protects TR_1 from excessive reverse V_{BE}.

Note (3). In order to provide approximately 90° phase shift, then

$$X_{C2} < \frac{R_1}{10}$$

Note (4). To provide approximate integration of the output waveform, then $C_3R_{10} > 10t$ where $t = \frac{1}{f}$ and $R_L \gg R_{10}$.

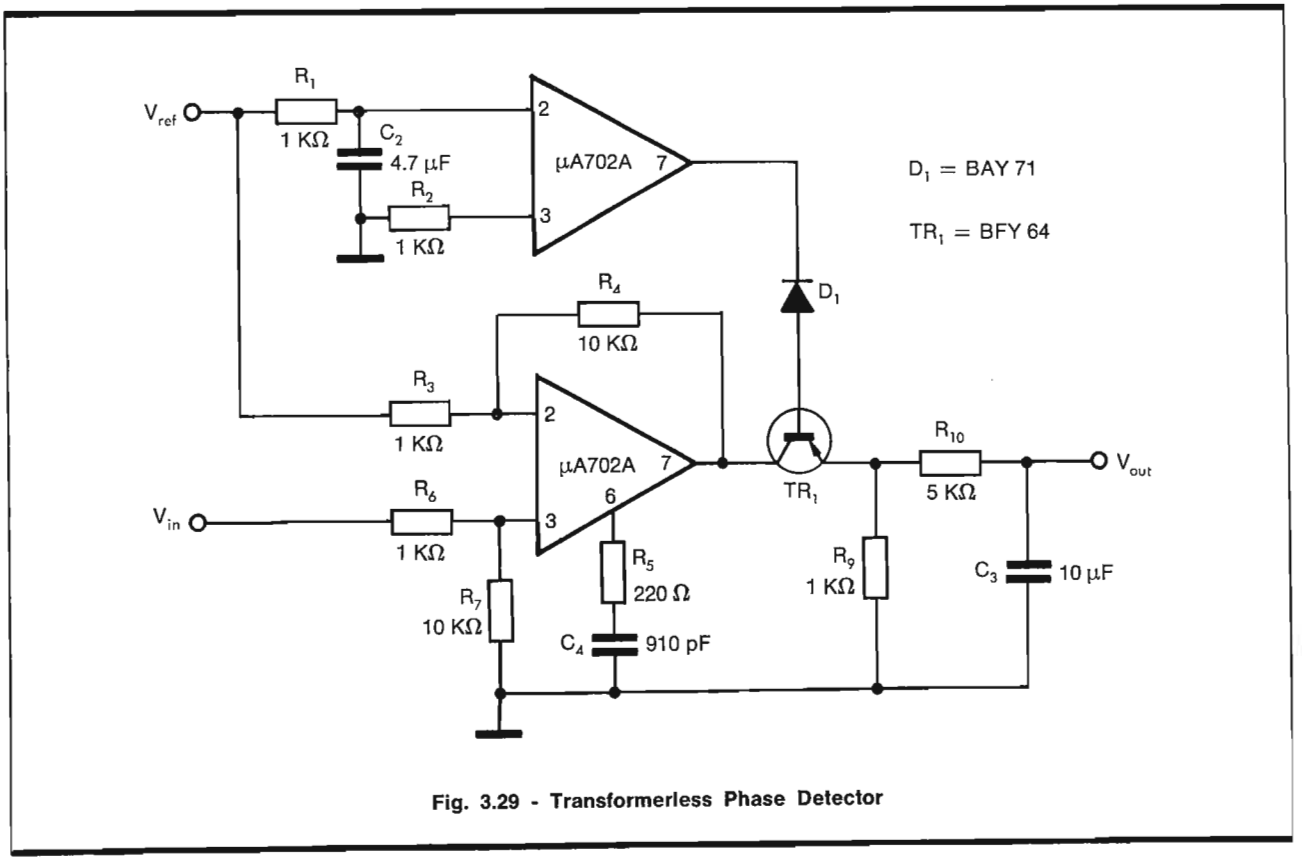


Fig. 3.29 - Transformerless Phase Detector

Note (5). Although the output is relatively independent of the ratio in amplitude between $V_{(Ref)}$ and $V_{(in)}$, optimum results will be obtained if these amplitudes are matched to within 10%. In any case, care must be taken to avoid exceeding the common-mode operating range of both amplifiers by limiting the input to a maximum of 1 V peak-to-peak.

Greater sensitivity may be obtained by increasing the gain of the differential amplifier (R_4 R_3, R_7 R_6) but it is important to avoid allowing the amplifier from operating non-linearly due to a combination of input error signals, otherwise the descrimination is upset.

3.3 μA709 BASIC AMPLIFIER CIRCUITS

3.3.1 Inverting Amplifier

Fig. 3.30 shows the amplifier circuit diagram of an inverting amplifier using the μA709 where the output voltage is input voltage dependent as shown by the following formula:

$$e_o = -\frac{R_2}{R_1} e_1$$

In this circuit the output impedance of the amplifier is reduced by means of feedback to values less than one ohm while the input impedance is:

$$Z_{in} = \frac{e_{in}}{I_{in}} = R_1$$

The stability versus frequency is obtained by R_4, C_1, C_2 groups designed to obtain the maximum bandwidth (0.5 MHz).

The circuit can obviously also operate with different resistance values and, in consequence, with different closed-loop gains.

It should be noted that offset noise and thermal drift indicate the minimum applicable signal, while the input current, noise current and bandwidth requirement limit the maximum resistances values.

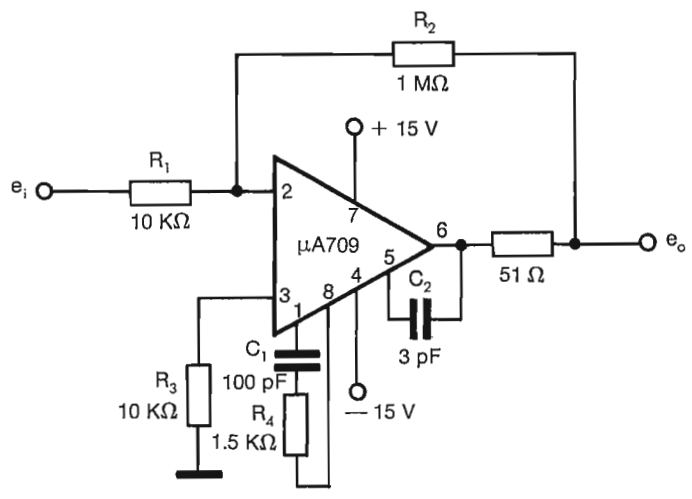


Fig. 3.30 - Inverting Amplifier

3.3.2 Non-Inverting Amplifier

The excellent differential characteristics, the high gain and high input voltage range of the μA709 make this device particularly suitable for non-inverting amplifier applications.

Fig. 3.31 shows an amplifier of this type made with the μA709 device whose gain is defined by the following equation:

$$e_o = \frac{R_1 + R_2}{R_1} e_1$$

The output impedance is lowered up to values of a fraction of an ohm by negative feedback, while the input impedance rises, as given by:

$$Z_{in} = \frac{1}{Y_{in}} = \frac{1}{Y_{3G} + Y_{23} \dfrac{1}{1 + \dfrac{A_o}{\dfrac{R_1 + R_2}{R_1}}}}$$

where Y_{3G} and Y_{23} are the admittances between input 3 and ground and inputs 2 and 3 respectively. Since the μA709 common admittance ($Y_{3G} = Y_{G2}$) is very low at low frequency, of the order of $10^{-8}\Omega^{-1}$ the input resistance is given by:

$$R_{in} = \frac{1}{Y_{23}} \left(\frac{R_1}{R_1+R_2} A_o \right)$$

Finally, the compensation network has been designed to obtain the maximum bandwidth, while the resistance R_s has been chosen equal to $R_1//R_2$ to minimise offset and drift.

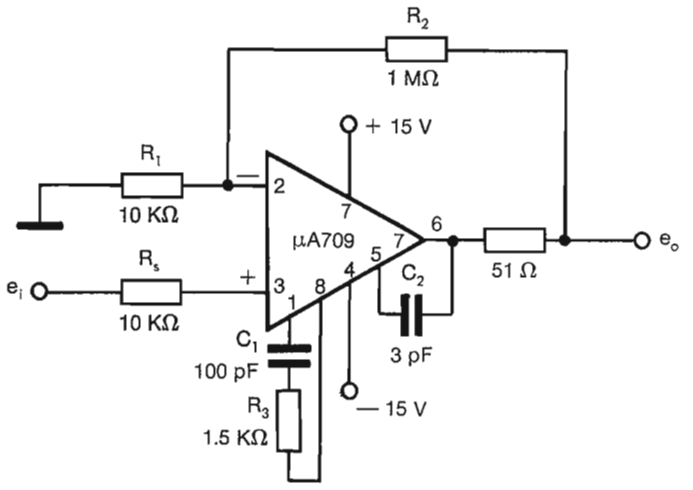


Fig. 3.31 - Non-Inverting Amplifier

3.3.3 Differentiator

Fig. 3.32 (a) shows the circuit diagram of a differentiator using the μA709 element.

The current flowing into the summing point through the capacitor C_d is defined by the equation:

$$i_c = C_d \frac{de_1}{dt}$$

Since the current i_c is equal to the feedback current flowing through resistor R_d (less the μA709 input current) the output voltage is given by:

$$e_o = -i_c R_d = -R_d C_d \frac{de_1}{dt} = -T_d p e_1$$

The circuit diagram shown in Fig. 3.32 (a) differs from the ideal differentiator by the addition of capacitor C_r and resistor R_i.

These components have been added to ensure the necessary frequency response stability to the differentiator circuit. More-over, limiting the gain measured at high frequencies obviously higher than the operating ones, the output noise can be drastically reduced.

Resistor R_i is inserted to limit the current across capacitor C_d, thus avoiding source overloads.

In addition, the circuit acts as a differentiator at low frequencies, an integrator at high frequencies and as a proportional amplifier at intermediate frequencies as indicated in Fig. 3.32 (b).

The differentiator time-constant is selected so that the maximum rate of change of input signal will produce full-scale output not higher than the maximum allowable e_{omax}:

$$R_d C_d = \frac{|e_o|_{max}}{\left| \frac{de_1}{dt} \right|_{max}}$$

Finally, the error produced by summing point voltage and current offset referred to the input is:

$$\left(\frac{de_1}{dt} \right) \text{error} = \frac{1}{C_d} \left(\frac{1}{R_d} e_{offset} + I_{offset} \right)$$

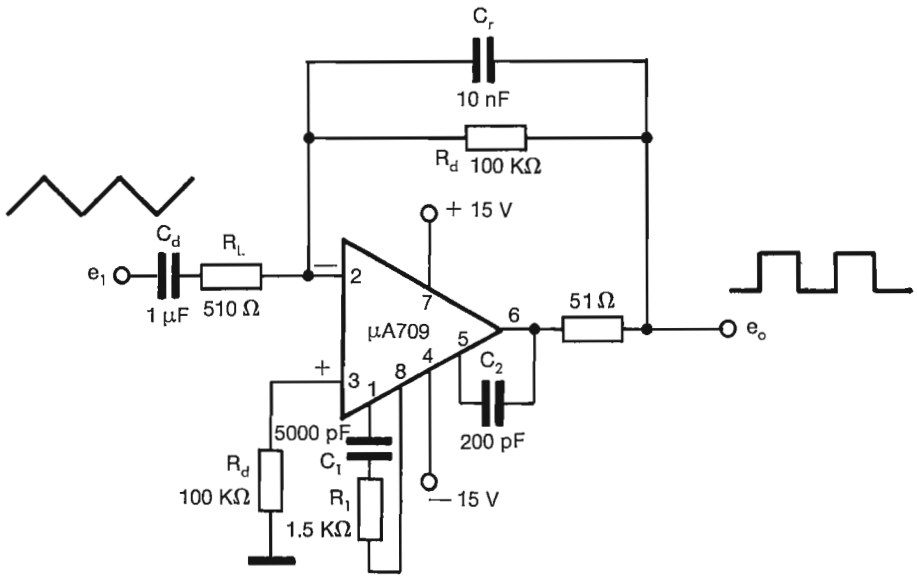


Fig. 3.32 (a) - Practical Differentiator

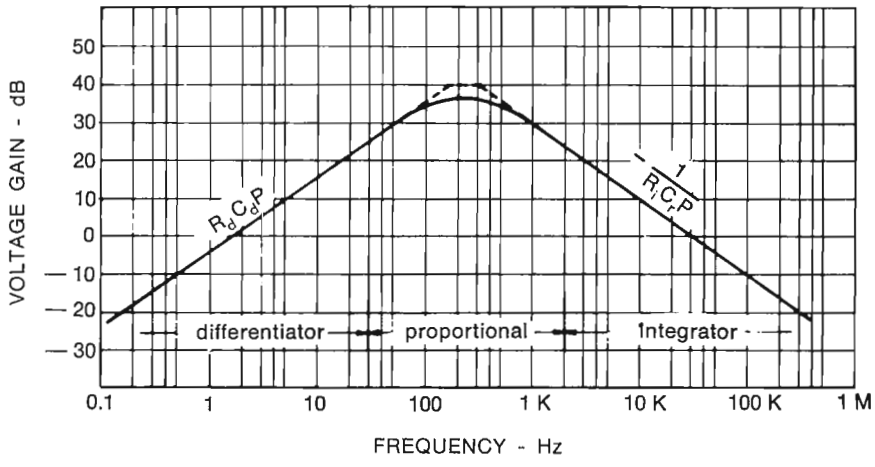


Fig. 3.32 (b) - Frequency response of pratical differentiator of fig. 3.32 (a)

3.3.4 Integrator

The capability of being able to execute the integral operation accurately is of fundamental importance in many applications.

The circuit in Fig. 3.33 shows a free-running integrator (i.e. without reset or hold circuits) made with a μA709 element.

Since the current e_1/R flowing across the input resistor must pass through the feedback capacitor, we obtain:

$$-C\frac{de_o}{dt} = \frac{e_1}{R}$$

and thus:

$$e_o = -\frac{1}{R_c}\int^{t} e_1 dt = -\frac{e_1}{pT}$$

where T = RC is the time-constant of the integrator. For example, in Fig. 3.33, R = 100 kΩ, C = 1 μF, RC = 0.1 sec.

T is really the time required for the output voltage to change by an amount equal to the average value of the input voltage during the time Δt:

$$-\Delta e_o = \frac{\Delta t}{T}\,\overline{e_i}$$

The circuit shown in Fig. 3.33 must be used in a closed-loop system and equipped with circuits capable of setting a starting condition at the output; in fact, due to its voltage and current offset the actual integration tends to reach one of its saturation limits within a certain time.

Finally, the R_1, C_1 and C_2 networks ensure the necessary frequency stability at the output.

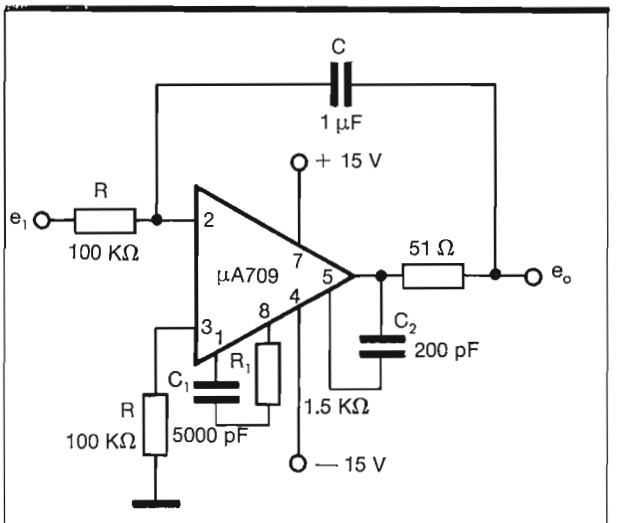


Fig. 3.33 - Integrator

3.3.5 Low Input Current D.C. Amplifier

In spite of the excellent input characteristics of the μA709 operational amplifier there are applications where better performances are required.

For instance, in logarithmic amplifiers with a higher swing than the one described in Section 3.4.5,

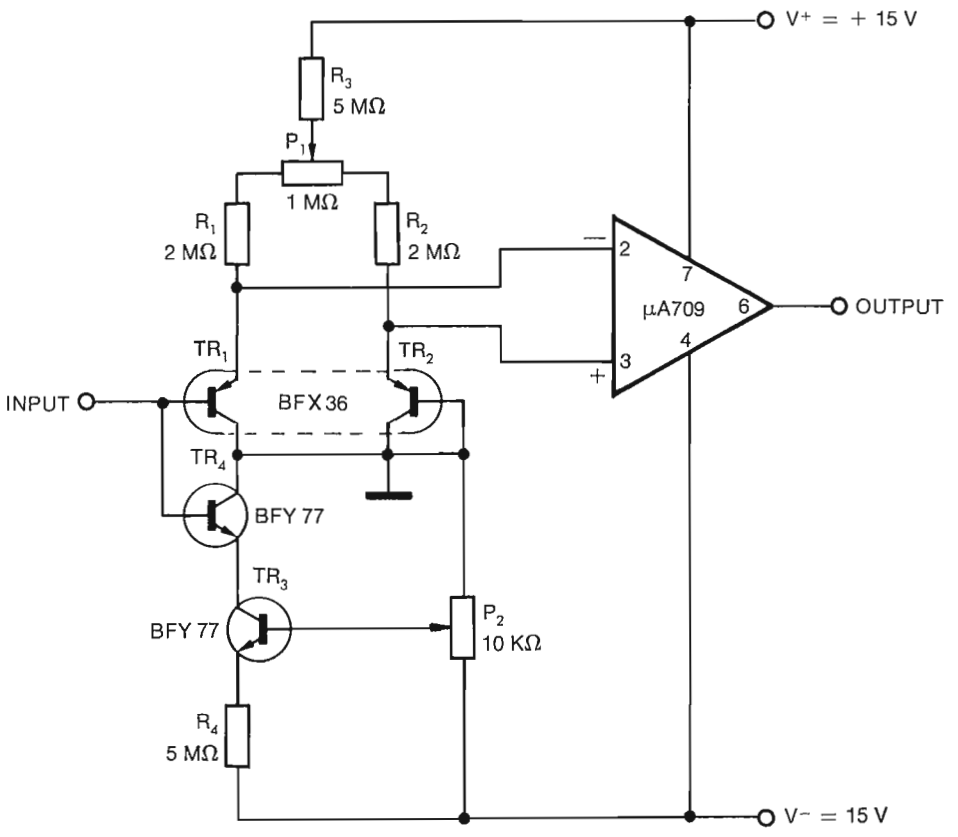


Fig. 3.34 - Low Input Current D.C. Amplifier

in summing amplifiers with high values of source resistance and in high-linearity and large time-constant integrators there is the need for improved input characteristics.

Fig. 3.34 shows the operational amplifier circuit diagram employing a μA709 element and a differential stage in a common-collector configuration, with a dual PNP transistor type BFX36.

In this amplifier the voltage drift is equal to the sum of the μA709 voltage drift and that of the input stage added to the μA709 current drift multiplied by the output impedance of the common-collector stage.

The adaptor stage operates with a very low collector current (1μA) and practically zero collector-base voltage.

This is the reason why the influence of the I_{CBO} of the transistors is eliminated, and the current drift is due to current gain variations with temperature.

The amplifier has a high input impedance (15 MΩ) and a small input current (5-10 nA).

The input current at ambient temperature can become zero by the current generator comprising TR_3 and transistor TR_4 which are complementary to TR_1: in fact by adjusting potentiometer P_2 it is possible to alter the current of TR_3 and consequently that of TR_4 in order that:

$$I_{b4} = \frac{I_{C4}}{h_{FE4}}$$ be equal to the base current

or TR_1 which is $I_{b1} = \dfrac{I_{C1}}{h_{FE1}}$

Moreover it is possible to obtain a current drift improvement within a limited temperature range (O to 60°C); in fact a typical current drift value is 20 pA/°C.

An improved increase in D.C. stability is obtained by keeping the temperature of the whole amplifier constant, this is possible due to its small dimensions. Note (1). Potentiometer P_1 is used to adjust the voltage offset with the input short-circuited to ground.

3.3.6 Power Booster Amplifier

The output power of the μA709 operational amplifier is satisfactory for most applications but insufficient to drive resistive and capacitive loads requiring more than a few milliamperes.

Greater output power may be obtained by adding a unity voltage gain power booster, in cascade with the integrated amplifier — within the feedback loop.

Fig. 3.35 (a) shows the block schematic of the complete amplifier when the booster is connected as the output stage of the μA709, all the supply decoupling components are shown, together with suitable compensating networks for the amplifier.

The integrated amplifier determines the input conditions, bandwidth and slewing rate while the output characteristics derive from the booster.

Fig. 3.35 (b) shows the power booster circuit. Two difectly-coupled voltage amplifier stages in cascade drive the complementary output stage. The output is connected back to the emitter of the first stage, and gives 100% negative feedbak to maintain the voltage gain at unity, increases the input impedance and improves the bandwidth.

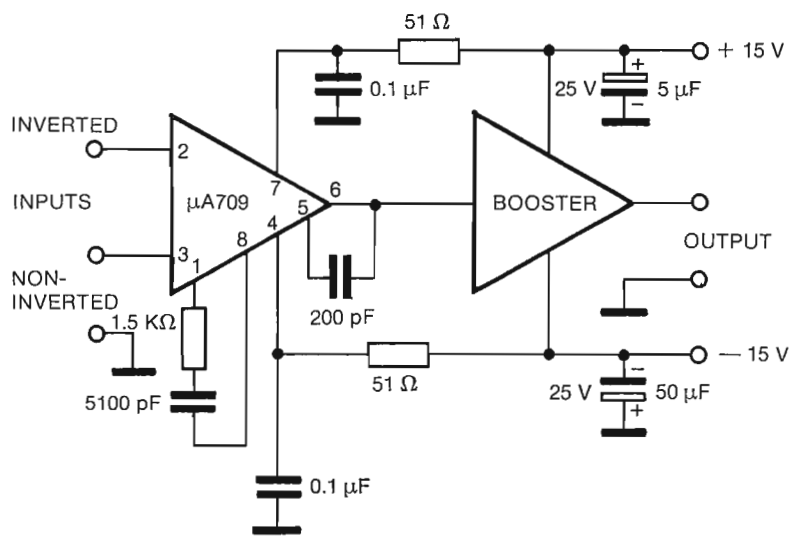


Fig. 3.35 (a) - Block Schematic of Operational Amplifier and Power Booster

The booster under consideration, protected up to a maximum ambient temperature of 50°C, against a permanently short-circuited output for all input signals, allows an output voltage swing of ± 10 V to be obtained with a load of 100 Ω.

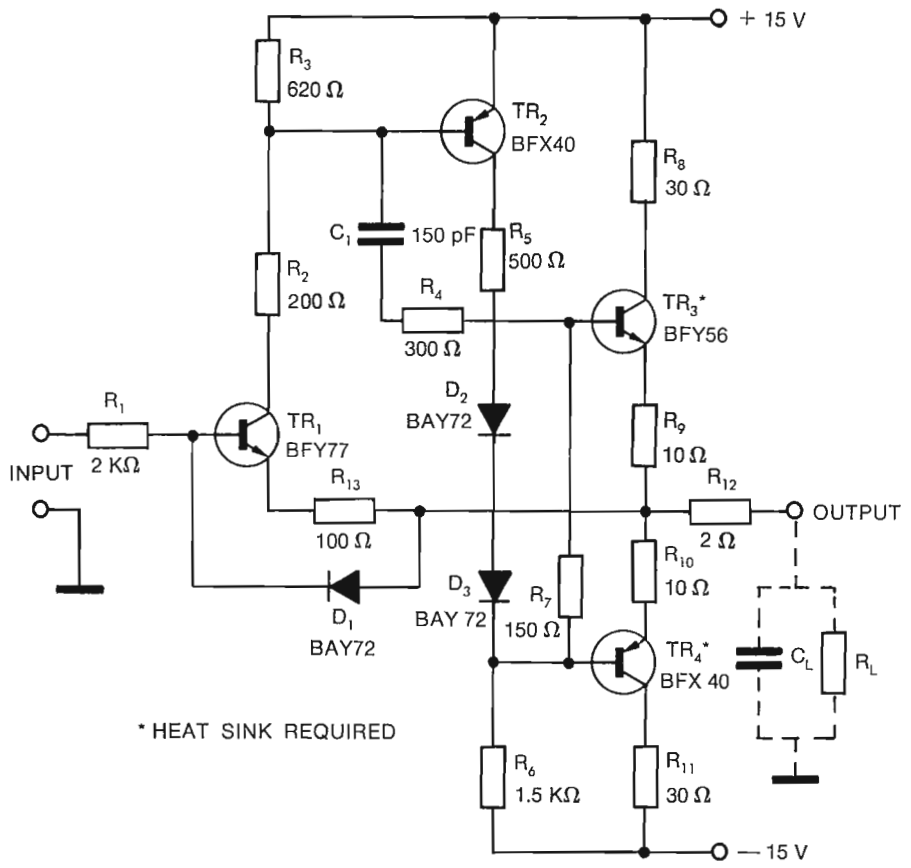


Fig. 3.35 (b) - The Power Booster Circuit Diagram

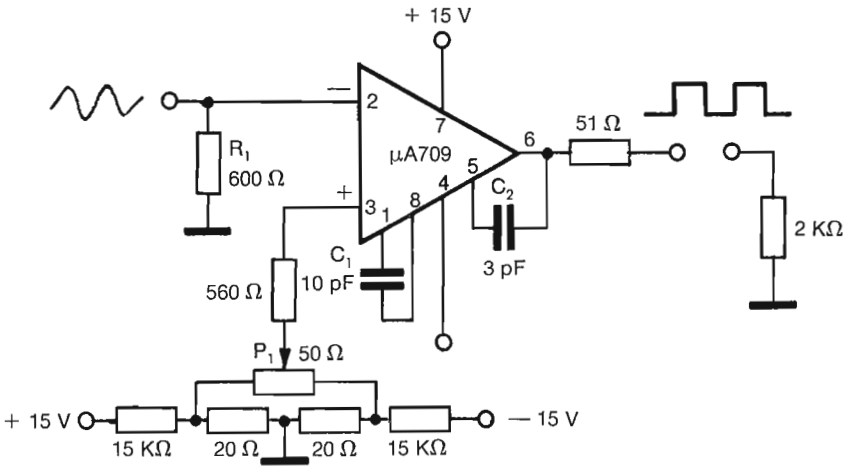


Fig. 3.36 (a) - Squarer

3.4 MISCELLANEOUS CIRCUITS

3.4.1 Squarer

Fig. 3.36 (a) shows a low-frequency squared using the high performance μA709 element.

The input impedance is governed, to within a few percent, by the resistor R_1 in parallel with the non-inverting input since the input intrinsic resistance of the μA709 remains fairly high at each operating condition.

The maximum input level is limited at ± 5 V zero-to-peak (= + 13 dBm) by the breakdown voltages of the input transistor base-emitter junctions.

Fig. 3.36 (b) shows the limiting characteristic with a sinusoidal input signal at a frequency of 1 KHz where the output voltage has been measured with a true root-mean-square voltmeter.

Potentiometer P_1 is used to adjust the offset voltage to zero and to produce a symmetrical square-wave at the output, with the minimum input signal (— 55 dBm).

Under such conditions the squarer can operate for signals between — 55 dBm and + 10 dBm, keeping the square wave at the output symmetrical to within 1% accuracy.

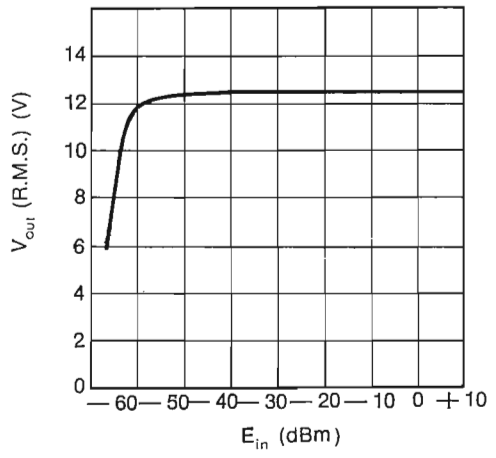


Fig. 3.36 (b) - Squarer Limiting Characteristics

3.4.2 Comparator

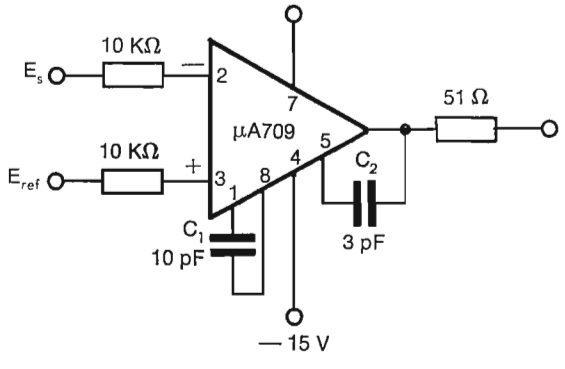
The μA709 integrated amplifier can be used as voltage comparator, particularly at low frequency, as shown Fig. 3.37 (a). The reference and input voltages must not exceed the maximum allowable limits for both common and differential signals which can be applied to the input.

The integrated amplifier is used in open-loop configuration with the compensating networks designed for the minimum values.

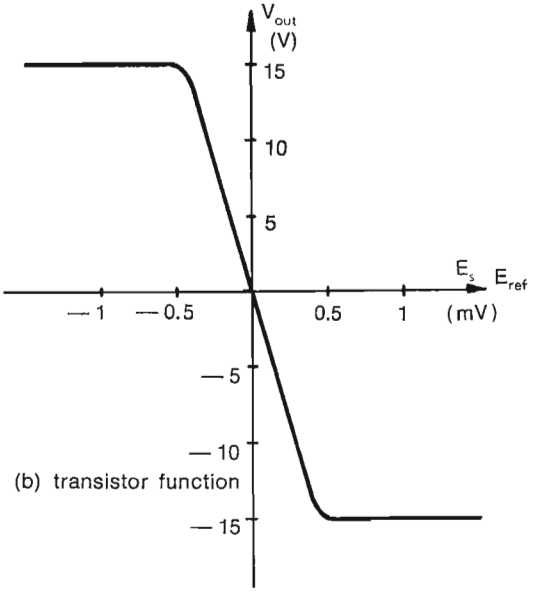
The input-output transfer function is shown in Fig. 3.37 (b); note the low transition voltage.

The curve corresponds to the condition in which the offset voltage has been set to zero, otherwise the transfer function will remain within the limits of ± 5 mV of the input voltage.

Since voltage comparators are often used to measure the difference between a square wave and the reference voltage, switching times are important.



(a) circuit



(b) transistor function

Fig. 3.37 - Voltage Comparator

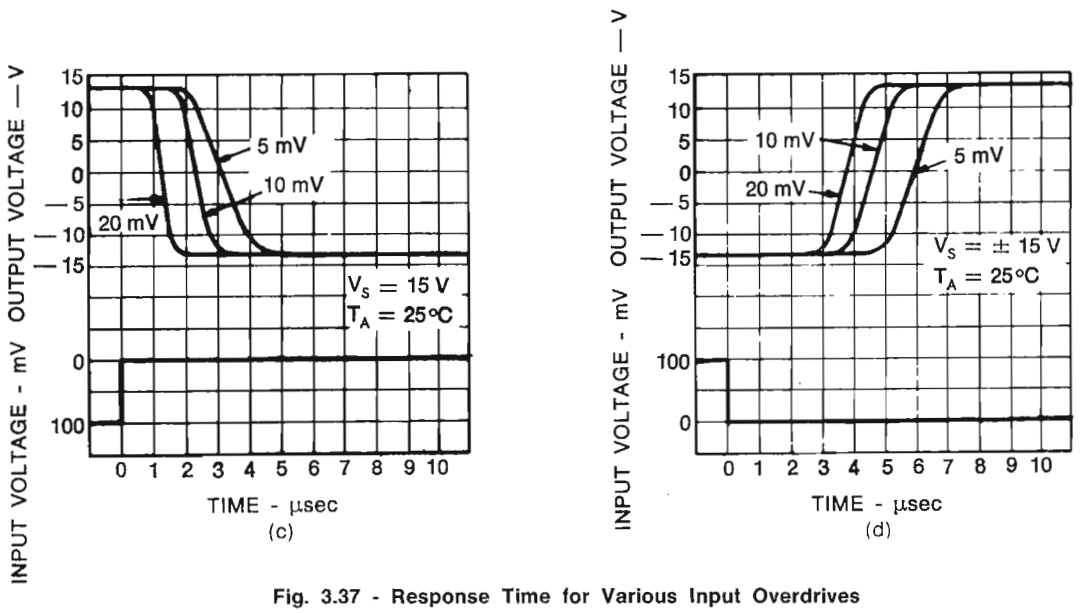


Fig. 3.37 - Response Time for Various Input Overdrives

The comparator response times for output voltages which vary negatively or positively, are shown in Fig. 3.37 (c) and in (d) for different values of overdrive voltages (for response-time definition refer to the μA710 data sheet).

The comparator output can be kept compatible with digital integrated circuits using the circuit shown in Fig. 3.37 (e) and (f) where the resistor R = (510 Ω) limits the μA709 output current.

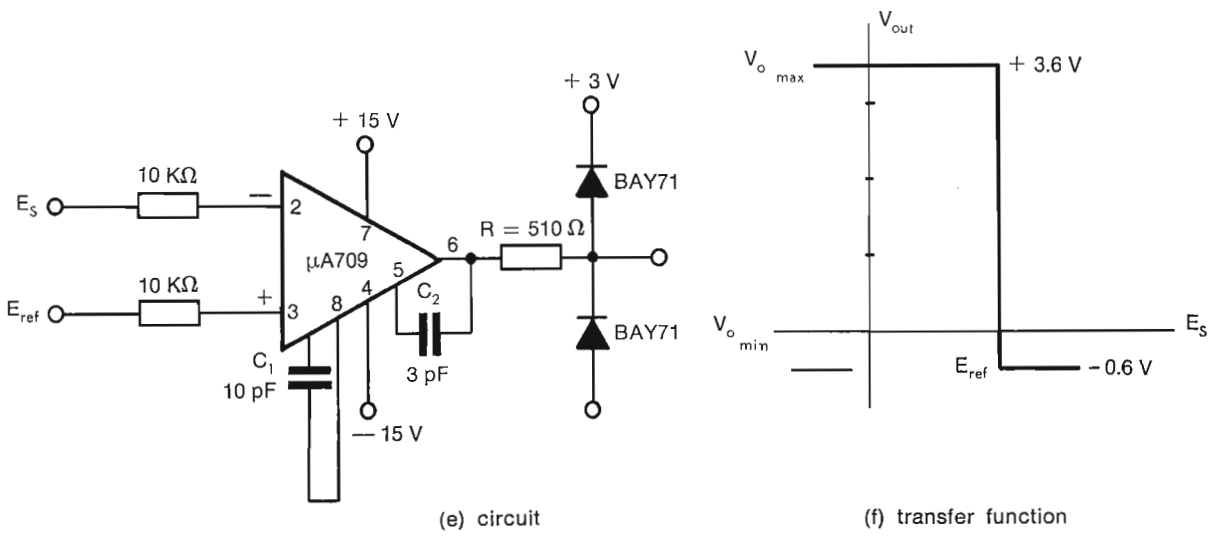


Fig. 3.37 - Voltage Level Detector

3.4.3 Voltage Comparator with Hysteresis

For applications where a certain amount of noise is superimposed it is desiderable to have a certain hysteresis in the transfer characteristic.

The hysteresis is obtained by means of positive feedback applied between output and input.

These comparators are also useful in all cases where the input signal varies very slowly.

In fact, for the hysteresis comparator, the time to change from one state to the other is independent, as a first approximation , of the input signal; for the comparator described in paragraph 3.4.2 the time

necessary to change from one state to the other is strictly dependent on the rate of change of the input voltage.

Fig. 3.38 shows a comparator with a hysteresis cycle using the μA709 arranged in order to have the output compatible with integrated digital circuits.

The hysteresis cycle V_H is given by:

$$V_H = \frac{\Delta V_o}{A_C} \cong \Delta V_o \beta$$

where:

$$\beta = \frac{R_1}{R_1 + R_2}$$

and:

$$\Delta V_o = V_{o\,max} - V_{o\,min}$$

By the use of the μA709 element, comparators which are sufficiently accurate with a hysteresis cycle in the order of a few millivolts can be designed.

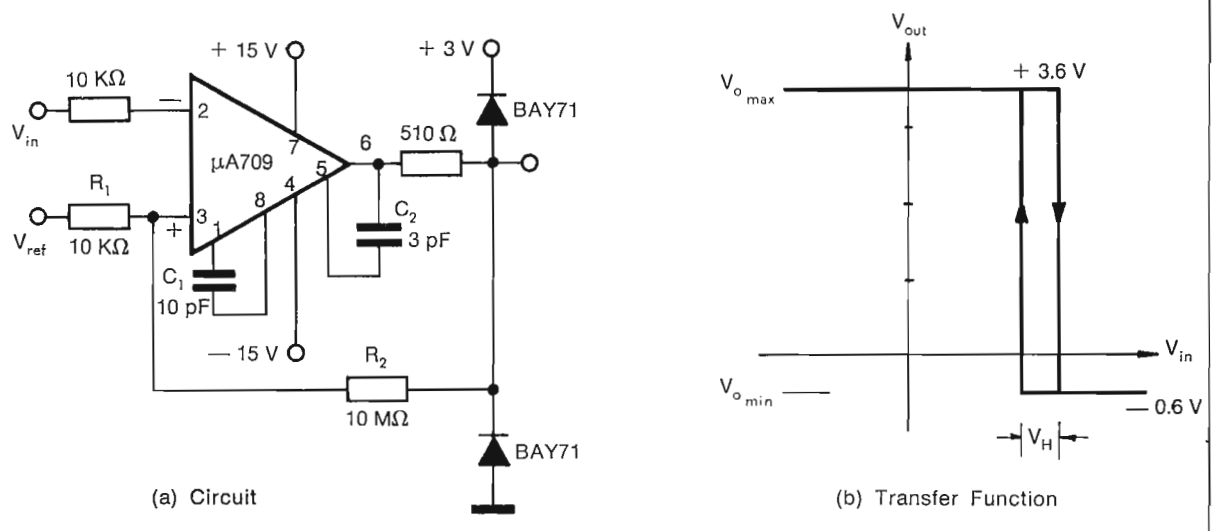


Fig. 3.38 - Level Detector with hysteresis

3.4.4 Astable Multivibrator

Fig. 3.39 (a) shows the circuit diagram of an astable multivibrator using the μA709 integrated amplifier.

The circuit has two states: in one the output is at positive saturation level, in the other at negative saturation level.

Assuming, for instance, that when starting, the μA709 output reaches the positive saturation level, this is due to the effects of positive feedback produced across the voltage divider R_1 and R_2, as the capacitor C across the resistor R is positively charged. When the inverting input voltage reaches the same value as the non-inverting input one, given by:

$$V^+_{o\,max} \frac{R_1}{R_1 + R_2}$$

the circuit switches very quickly to the negative saturation level.

In this new state the non-inverting input is kept at the voltage:

$$V^-_{o\,max} \frac{R_1}{R_1 + R_2}$$

Therefore the inverting input remains at the potential of the capacitor charged to the voltage:

$$V^+_{o\,max} \frac{R_1}{R_1 + R_2}$$

because the switching took place very quickly. The circuit therefore, remains at the negative state for the time necessary to discharge the capacitor and to charge it approximately to:

$$V^-_{o\,max} \frac{R_1}{R_1 + R_2}$$

through the resistor R.

The oscillation period is given by:

$$\tau = RC\log_e \frac{(V^+_{o\,max} - V^-_{o\,max}\beta)}{V^+_{o\,max}(1-\beta)} \cdot \frac{(V^-_{o\,max} - V^+_{o\,max}\beta)}{V^-_{o\,max}(1-\beta)}$$

where $\beta = \dfrac{R_1}{R_1 + R_2}$

which for a symmetrical output amplifier, is:

$$\tau = 2RC\log_e\left(1 + 2\frac{R_1}{R_2}\right)$$

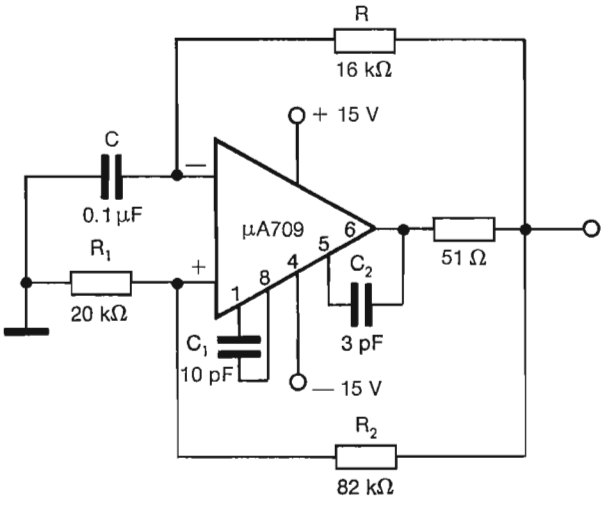
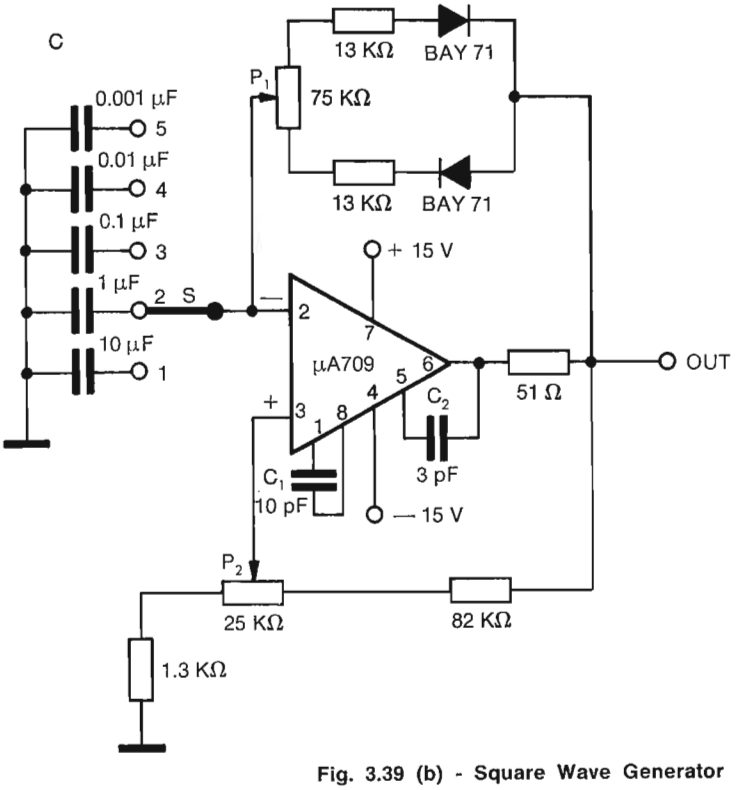


Fig. 3.39 (a) - Free Running Multivibrator



S position	f Hz
1	2-20
2	20-200
3	200-2 K
4	2 K-20 K
5	≥ 20 K

Fig. 3.39 (b) - Square Wave Generator

This multivibrator has excellent frequency stability characteristics (better than 1%o for supply voltages variations of a few percent).

Finally, Fig. 3.39 (b) shows a square-wave generator. The fine frequency adjustment is made by potentiometer P_1 which varies the hysteresis cycle, while the coarse adjustment is obtained by switching the capacitors C.

Potentiometer P_2 is used to vary square wave duty-cycle.

It should be noted that the multivibrator stability decreases by some percent by the addition of diodes and potentiometers.

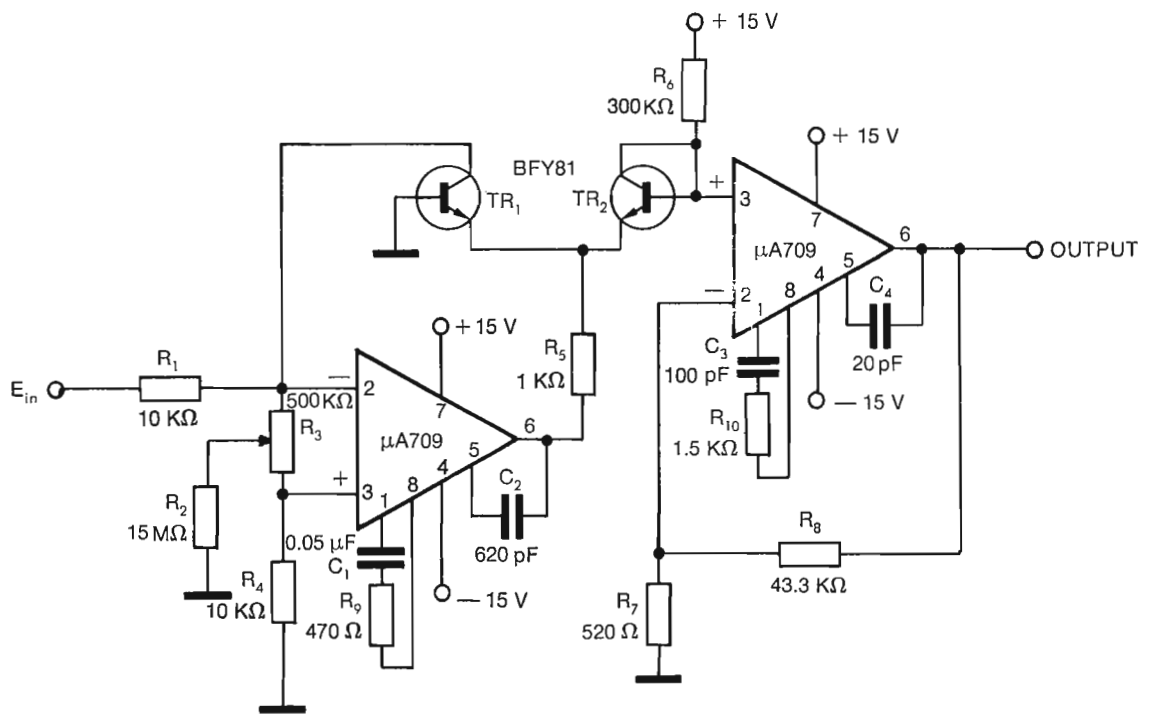


Fig. 3.40 (a) - Logarithmic Amplifier

3.4.5 Logarithmic Amplifier

The bipolar transistor is probably the most predictable non-linear element know to physics. In fact it is known that the variation in collector current with emitter-base voltage is given by

$$I_C \propto \exp\left(\frac{qV_{BE}}{kT}\right) \qquad \ldots\ldots\ldots\ldots\ldots (1)$$

where $V_{BE} > \frac{4kT}{q}$

In this equation, q is the charge of an electron, k is Boltzmann's constant and T is the absolute temperature. The expression holds up to high currents where emitter contact and base spreading resistances become important and down to low currents where collector leakages cause inaccuracy. The expression is valid for operation over at least nine

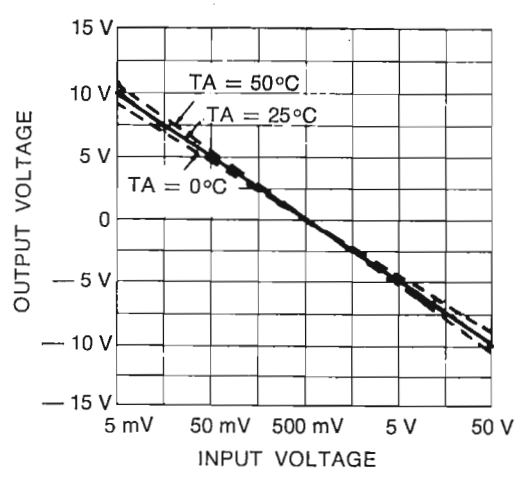


Fig. 3.40 (b) - Logarithmic Amplifier

decades of collector current with well-made silicon transistors. This contrasts with similar expressions for diode current and the emitter current of transistors which show substantial error over three decades of current operation.

Using the expression given above, it can be shown that the emitter-base voltage differential between two matched transistors operating at different collector currents is

$$\Delta V_{BE} = \frac{kT}{q} \log_e \frac{I_{C1}}{I_{C2}} \qquad \ldots\ldots\ldots (2)$$

In the circuit of Fig. 3.40 (a), a transistor TR_1 is used as the feedback element around a μA709 operational amplifier. The negative feedback forces the collector current of TR_1 to be equal to the current into the summing node of the amplifier. Hence, we can write

$$I_{C1} = \frac{E_{in}}{R_1} \qquad \ldots\ldots\ldots\ldots (3)$$

The collector current of TR_2 is determined by the positive supply voltage and R_6 as

$$I_{C2} = \frac{V^+}{R_6} \qquad \ldots\ldots\ldots\ldots (4)$$

If TR_1 and TR_2 are a matched pair of transistors, Eq. (2) can be used to give

$$\Delta V_{BE} = \frac{kT}{q} \log_e \left(\frac{R_6 E_{in}}{R_1 V^+} \right) \qquad \ldots\ldots\ldots (5)$$

Since the base of TR_1 is grounded, the negative of this voltage is presented to the input of the second amplifier. The gain of this stage is

$$A_V = \frac{R_7 + R_8}{R_7}$$

so

$$E_{OUT} = \frac{kT(R_7+R_8)}{q\,R_7} \log_e \frac{R_6 E_{in}}{R_1 V^+} \qquad \ldots\ldots\ldots (6)$$

which shows that the output voltage is proportional to the logarithm of the input voltage. It can be seen from Eq. (6) that the coefficient of the log term is proportional to absolute temperature, which gives it a thermal sensitivity of 0.3%/°C. The overall transfer function of the amplifier is given for various operating temperatures in Fig. 3.40 (b). As shown, the amplifier has an 80 dB dynamic range.

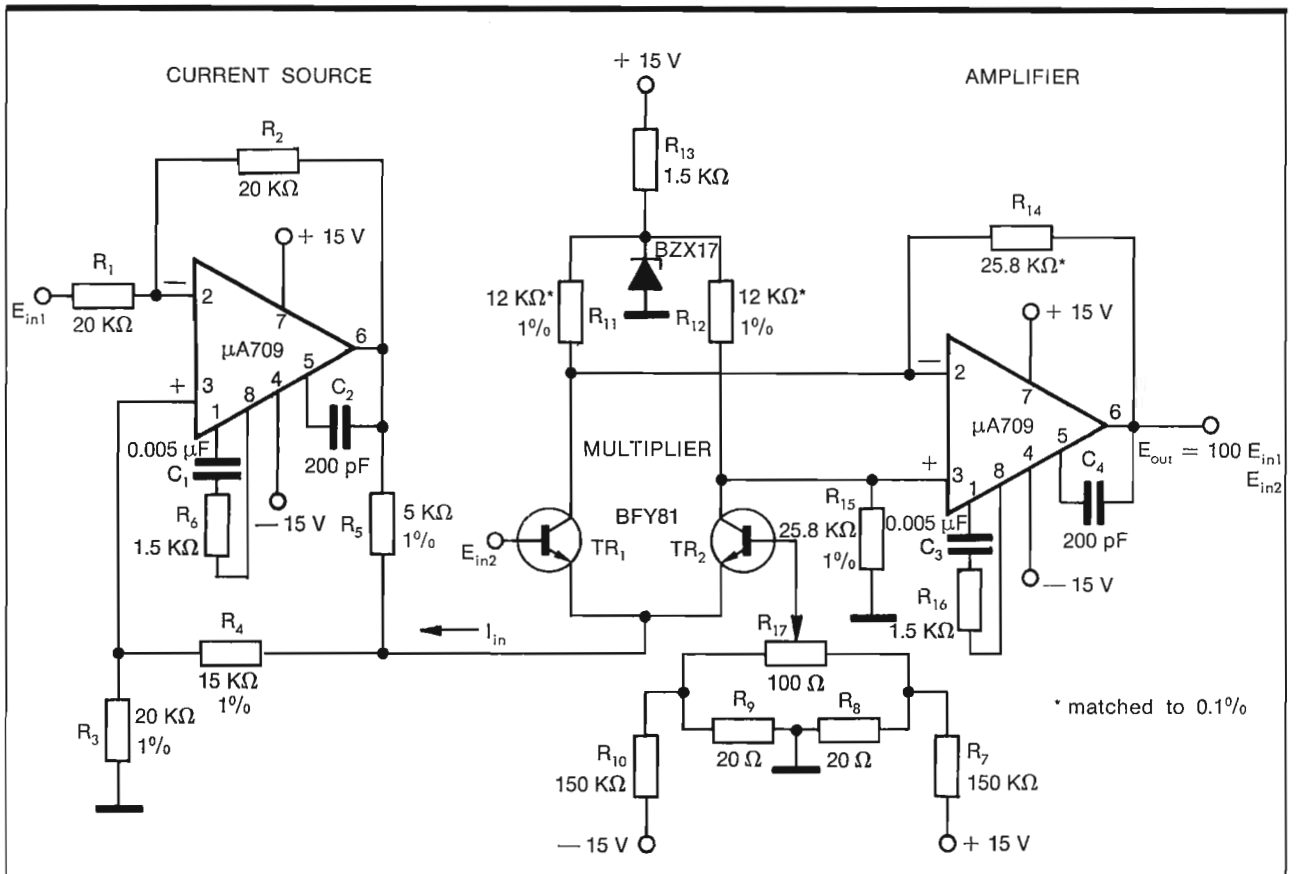


Fig. 3.41 - Multipler

Additional details of the circuit in Fig. 3.40 (a) are that R_2 and R_3 are used to provide an offset adjustment, which increases the dynamic range for small input signals. R_5 is used to limit the loop-gain of the input amplifier so that it can be frequency compensated. R_7 is chosen to be equal to the diode impedance of TR_2 to minimise the effect of the input bias current of the output amplifier. The slope of the log characteristic is determined by R_8 while R_6 determines the zero crossing.

3.4.6 Multiplier

Another interesting use for the non linear properties of the bipolar transistor is the multiplier shown in Fig. 3.41. The basic multiplying element is the transistor pair, TR_1 and TR_2. Its operation can be understood from the following:

The small signal transconductance of a transistor is given by:

$$\frac{dI_C}{dV_{BE}} = \frac{qI_C}{kT} \qquad \text{..... (1)}$$

A matched transistor pair in a differential configuration as shown in Fig. 3.41 will now be considered. For zero differential input voltage, the input current supplied to the emitters will split equally between the two transistors and the differential output current will be zero. Hence, Eq. (1) can be rewritten in terms of the differential output current, the input current to the emitters, and the input voltage as

$$I_{OUT} = \frac{q}{2kT} I_{IN} I_{IN2} \qquad \text{..... (2)}$$

Hence, the differential output current is proportional to the product of the differential input voltage and the current supplied to the emitters.

In Fig. 3.41, the first μA709 supplies a current that is proportional to a positive input voltage to the emitters of TR_1 and TR_2. Using standard operational amplifier theory, this current can be shown to be

$$I_{IN} = \frac{E_{IN1} R_2}{R_5 R_1} \qquad \text{..... (3)}$$

A second input voltage is supplied to the differential pair. Combining Eqs. (2) and (3) and setting $R_1 = R_2$ the output current of the differential pair is

$$I_{OUT} = \frac{q}{2kTR_5} E_{IN1} E_{IN2} \qquad \text{..... (4)}$$

The output of the pair is connected to a second μA709 that converts the differential current to a single-ended, zero referred voltage.

The output voltage of this amplifier will be $E_{out} = R_{14} I_{out}$, for $R_{14} = R_{15}$ and $R_{11} = R_{12}$. Hence,

$$E_{out} = \frac{qR_{14}}{2kTR_5} E_{IN1} E_{IN2} \qquad \text{..... (5)}$$

which shows that the output voltage is proportional to the product of the two input voltages.

There are several hints that are pertinent to making the circuit work right. One is that the resistor pairs R_{11}, R_{12} and R_{14}, R_{15} must be very closely matched (within 0.1 percent). An adjustment is provided for nulling the offset of TR_1 and TR_2. This adjustment should be made when the current-source current is at its maximum value. It should also be noted that Eq. (2) is a small-signal approximation, so the voltage input to the differential pair should be kept small. Restricting the input voltage to ± 20 mV gives linearity that is acceptable for the majority of applications. It should also be pointed out that E_{IN2} can be a bipolar signal while E_{IN1} must be a positive voltage.

3.4.7 Microammeter

Fig. 3.42 shows the circuit diagram of a low voltage-drop microammeter using the μA709.

The minimum scale (1μA) is essentially determined by the errors of the amplifier due to the thermal drift and, to a lesser degree, by the low frequency fluctuation and by the maximum allowable voltage drop at the meter terminals (3 mV).

The current through the indicating instrument is extremely accurate due to the high gain of the μA709, and is given by the following:

$$I_o = I_{IN} R \frac{R_1 + R_2}{R_1 R_L} = I_{IN} \frac{R}{3}$$

A 1 mA f.s.d. meter has been used as an indicating instrument in order to make the unit very sturdy.

Potentiometer P_1 is used for zero adjustment in order to compensate for the amplifier offset.

The meter, of very compact construction, is supplied with two batteries of 9 V and the current consumption is kept within very close limits (3 mA). Diodes D_1 and D_2 protect the amplifier and the different meter ranges are set from 1 μA to 100 mA, by means of the the switched input resistors.

The meter has an accuracy of 1% at ambient temperature, this is mainly determined by the quality of the meter, the tolerances of the resistors and with temperature, and has an accury of 0.2%/°C.

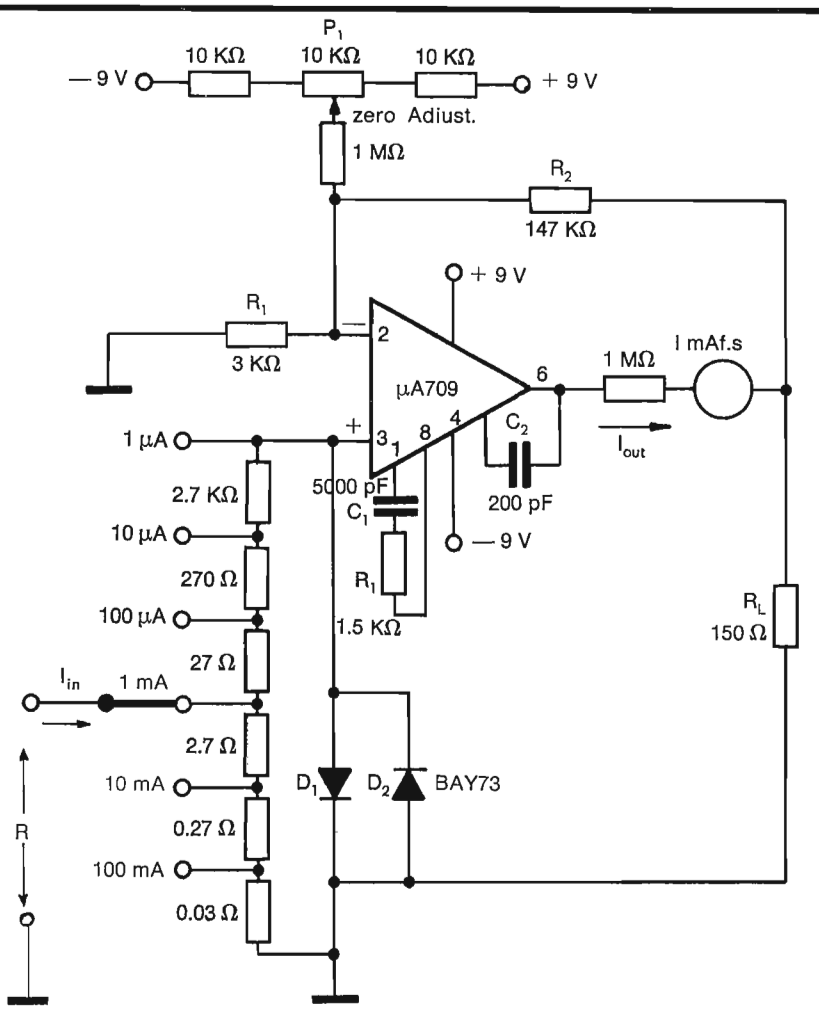


Fig. 3.42 - D.C. Microammeter

3.5 μA710 BASIC COMPARATOR CIRCUITS

3.5.1 Simple Voltage Level Detector

Fig. 3.43 (a) shows a basic circuit for using the differential comparator. A reference voltage between ± 5 V is connected to one input and the signal is fed into the other. When the input exceeds the reference signal, the output changes in state, see Fig. 3.43 (b). The output will switch positively or negatively depending upon how the inputs are connected.

This circuit has a variety of uses. It can be employed as a high-noise immunity buffer for transference from high level pulse circuits into low level integrated logic. Noise immunities as high as 5 V can be obtained and held within a few millivolts over worst-case conditions. Furhermore, the noise immunities of entire banks of line receivers can be controlled with a single voltage adjustment. Other uses are as a voltage comparator in analogue/digital converters, where one input is driven by the input signal and the other by a ladder network. The device has sufficient input sensitivity and output drive to be used directly as a tape or drum memory sense amplifier and threshold detector. Pulse shape restoration may also be carried out where the threshold level must be accurately maintained.

Note (1). In order to minimise offset voltage and thermal drift, the source resistance of the signal voltage and the reference voltage should be equal. These resistances should also be made as low as possible, preferably less than 200 Ω for best performance.

Note (2). Although the input voltage range of the μA710 is ± 5 V, the maximum voltage between the inputs is also ± 5 V. If one of the inputs is at + 5 V, for example, the other can only be driven as low as ground potential without exceeding the differential input voltage limit. It is important to observe this maximum rating since exceeding the differential input voltage limit and drawing excessive current in breaking down the emitter-base junctions of the input transistors could cause gross degradation in the input offset current and input bias current.

Note (3). Some attention to power supply bypassing

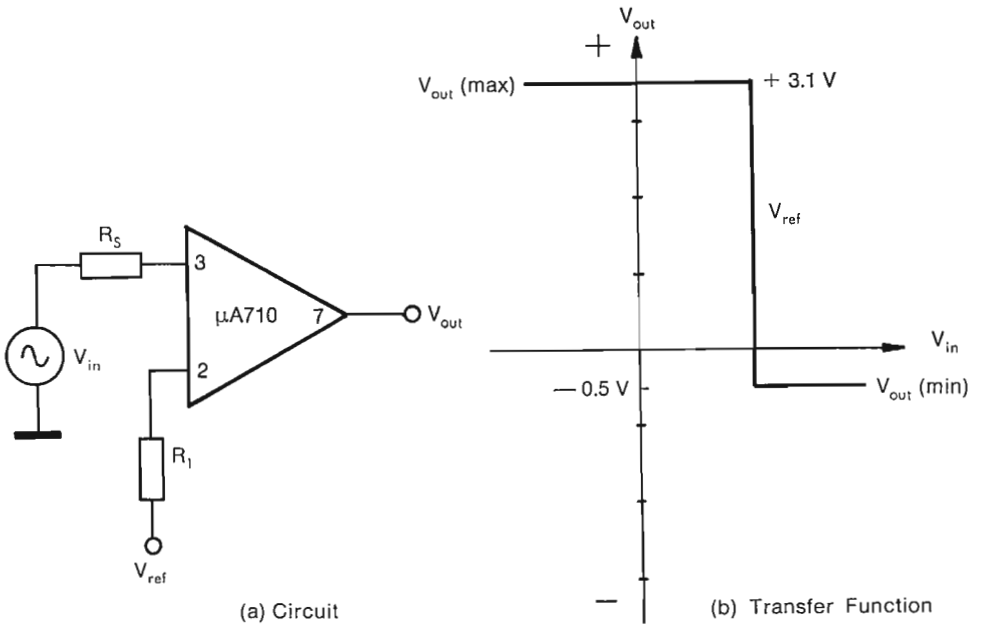


Fig. 3.43 - Simple Voltage Level Detector

is required with the μA710. This device is a multi-stage amplifier with gain to several hundred megacycles. Long, unbypassed supply leads or sloppy layouts can therefore cause oscillation problems. Bypassing with electrolytic or tubolar paper capacitors is ineffective. What is recommended is that both the positive and negative supplies be bypassed to ground using low-inductance, disc-ceramic capacitors (0.01 μF) located as close as practical to the device. A neat physical layout, keeping the input away from the output, is also important.

3.5.2 Voltage Level Detector with Hysteresis

In some applications where there are large amounts of noise on the signal when it is passing through the threshold of a level detector, it is de-

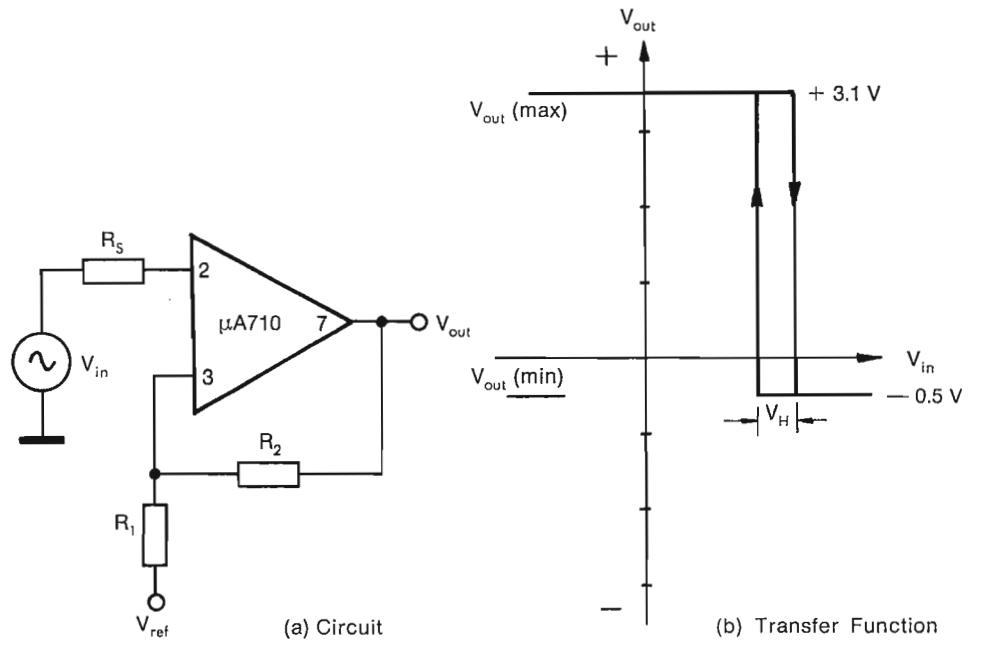


Fig. 3.44 - Voltage Level Detector with Hysteresis

sirable to have some hysteresis in the transfer characteristic. The hysteresis is generally made somewhat greater than the maximum expected noise. A circuit for producing hysteresis is shown in Fig. 3.44 (a). An external, positive feedback arrangement (R_2) is used.

The upper and lower trip points of this circuit can be written as follows:

$$V_{UT} = V_{ref} + \frac{R_1 (V_{out(max)} - V_{ref})}{R_1 + R_2} \quad \ldots\ldots (1)$$

and

$$V_{LT} = V_{ref} + \frac{R_1 (V_{out(max)} - V_{ref})}{R_1 + R_2} \quad \ldots\ldots (2)$$

Therefore, the hysteresis is

$$V_H = V_{UT} - V_{LT}$$

$$= \frac{R_1 (V_{out(max)} - V_{out(min)})}{R_1 + R_2} \quad \ldots\ldots\ldots\ldots\ldots (3)$$

The minimum amount of hysteresis obtainable is determined by the forward gain and output swing of the comparator.

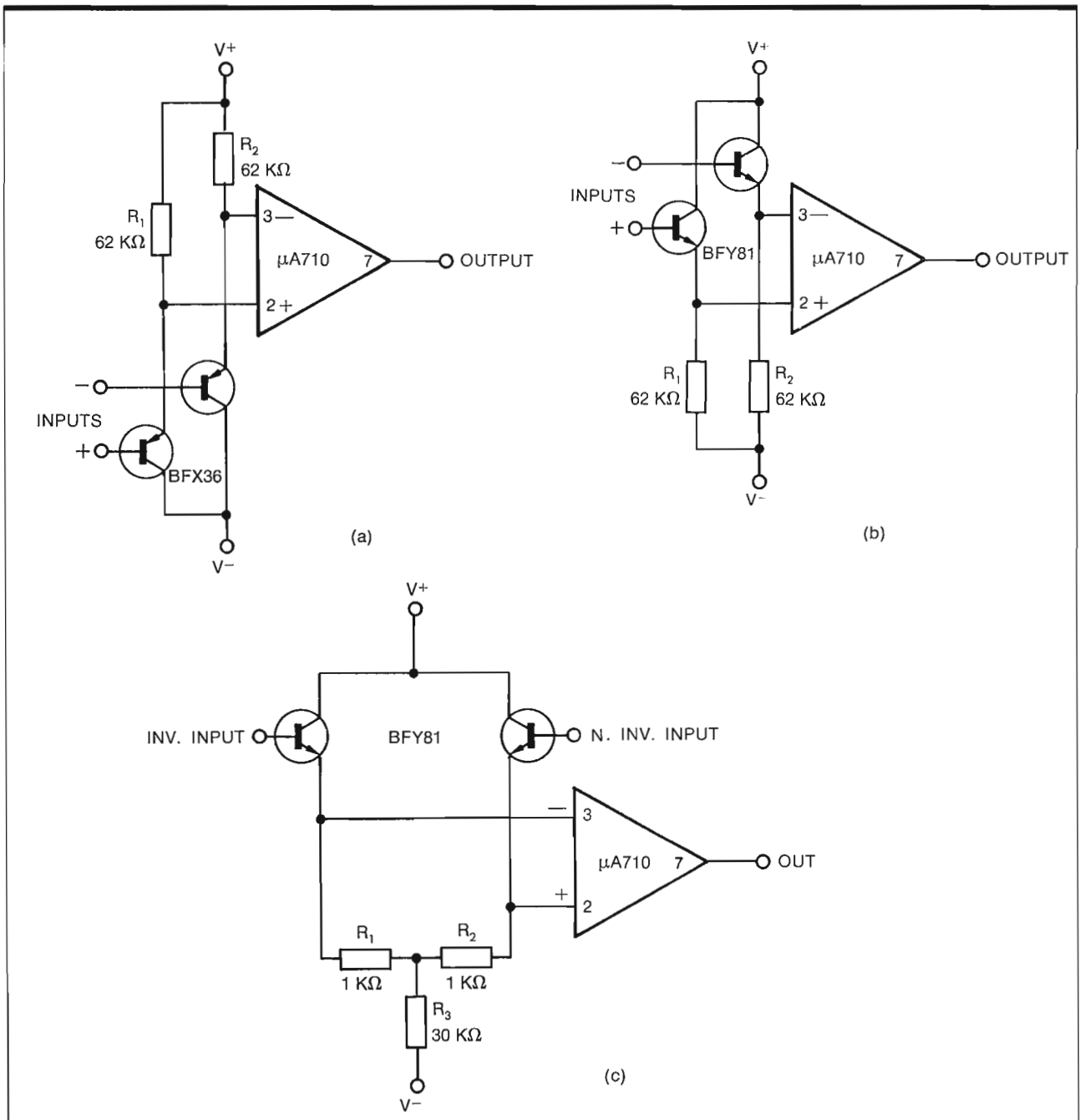


Fig. 3.45 - Circuits for obtaining a higher input resistance

It should not be made less than about 5 mV or oscillation will occur on the positive portion of the transfer function, if the small signal gain of the comparator is not greater than the ratio of the feedback resistors. Reduced hysteresis can usually be obtained when the comparator is used with logic circuits by taking the positive feedback from the output of the logic. The additional gain of the logic permits a smaller hysteresis. For example, with the additional gain of a DT L gate, it can be made less than 0.2 mV.

With the connection as shown in Fig. 3.44 (a) the μA710 can be substituted for a Schmitt trigger. it has the advantage, though, that non-zero trip points can be obtained and that both the upper and lower trip points are easily and independently adjustable over a wide range of positive and negative voltages.

Note (1). For a minimum offset and thermal drift

$$R_s \approx \frac{R_1 R_2}{R_1 + R_2}$$

3.5.3 Circuits used to obtain a higher input resistance

In a number of applications the input currents of the μA710 are sufficiently high to cause a significant error due to loading of the signal and reference voltage sources.

To overcome this, a transistor pair can be used in front of the comparator to reduce the input currents and increase the input resistance. Three possible circuits are given in Fig. 3.45. In the circuit (a) using the PNP pair the full input voltage range of ± 5 V is still available.

The NPN circuit (b) is quite satisfactory when the comparison is made at input voltages above — 2 V.

The third circuit (c) offers the advantage, with respect to the circuit (b), to maintain the same response time of the μA 710 element.

This is obtained keeping the maximum resistance seen by μA710 inputs equal to 2 kΩ.

It is possible to balance the comparator offsets in these circuits by unbalancing the emitter resistors (R_1 and R_2) on the input transistors.

The comparator speed is offset somewhat by the addition of the input stage. This is caused primarily by the collector-base capacitance of the input transistors loading the source.

The transistors shown in Fig. 3.45 were selected for a low collector-base capacitance as well as a high current gain, and should load the source with a total capacitance less than 10 pF.

3.5.4 Line Receivers

Frequently in the design of digital systems it is necessary to interconnect various equipments over long lines where the possibility of picking-up considerable noise exists. In the cases it is desirable to use a line receiver that has considerably more noise immunity than standard logic circuits to precondition the logic signals. Fig. 3.46 shows a line receiver using a μA710. The resistive divider on the input of the comparator permits higher level logic signals than are possible with the μA710 alone. It is also possible to put a capacitor at the comparator input (C_1) to make the circuit insensitive to fast noise spikes. Because of the high gain of the comparator, fast-rise output pulses can be obtained even with this integrating capacitor.

Note (1). For a minimum offset and thermal drift.

$$R_3 = \frac{R_1 R_2}{R_1 + R_2}$$

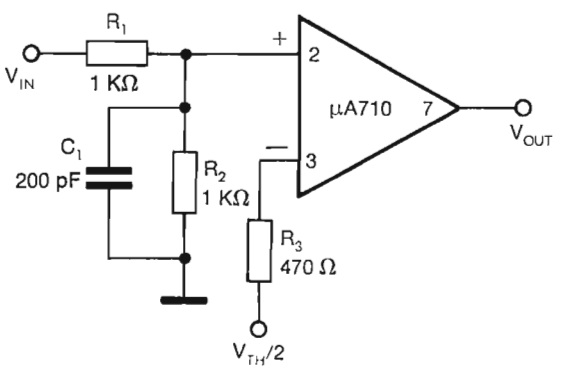


Fig. 3.46 - High Noise-Immunity Line Receiver for Slow High-Level Logic

3.5.5 Simple Window Discriminator

In many equipments, particularly automatic GO/NO-GO testers, it is necessary to determine if a voltage or pulse amplitude is within certain limits. A circuit for accomplishing this is shown in Fig. 3.47 (a). Two differential comparators are used. The lower-limit voltage V_1 is fed into the non-inverting input of one, and the upper limit voltage V_2 is fed into inverting input of the other. The two remaining inputs are connected together and driven with the signal.

Note (1). The relative values of the source resistance for the signal and the reference voltages should be

$$R_s = \frac{R_2}{2} = \frac{R_1}{2}$$

to make the accuracy dependent on offset currents rather than bias current. These resistances should also be as low as possible.

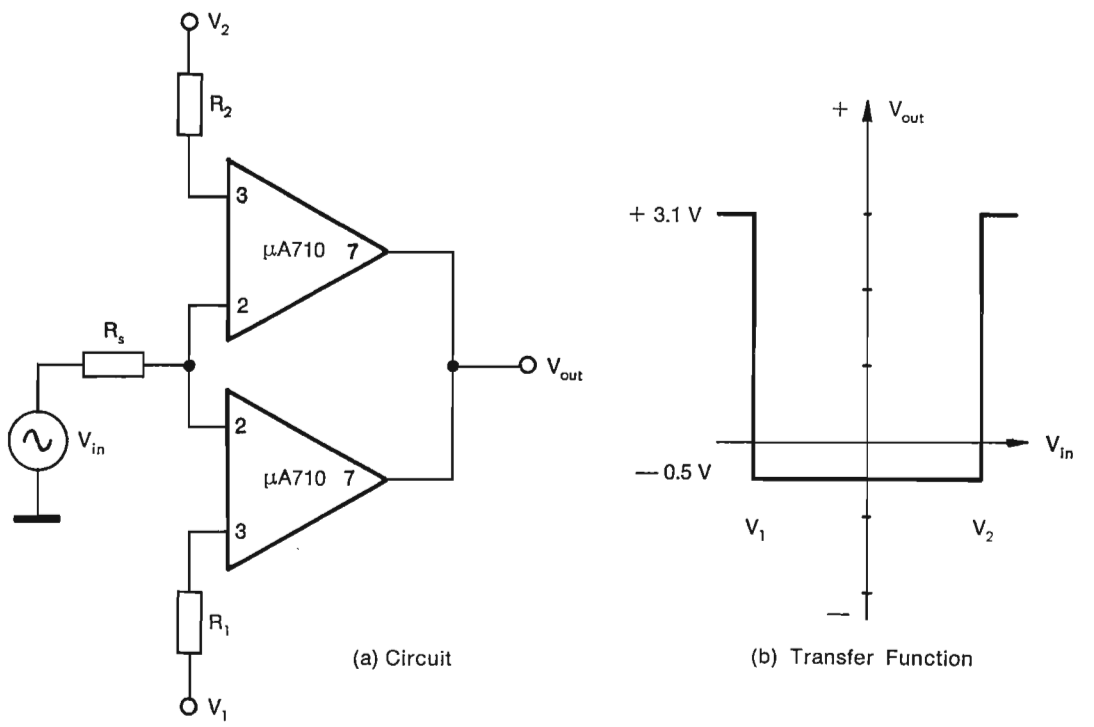


Fig. 3.47 - Simple Window Discriminator

3.6 MISCELLANEOUS CIRCUITS USING μA710

3.6.1 One-Shot Multivibrator

Fig. 3.48 shows a circuit using the μA710 as a precision, high-speed, one-shot multivibrator. It has the particular advantage over other types of monostable crcuits in that the trigger point can be quite accurately determined (± 10 mV) over a wide threshold voltage range (± 5 V).

A positive output pulse is obtained for a negative

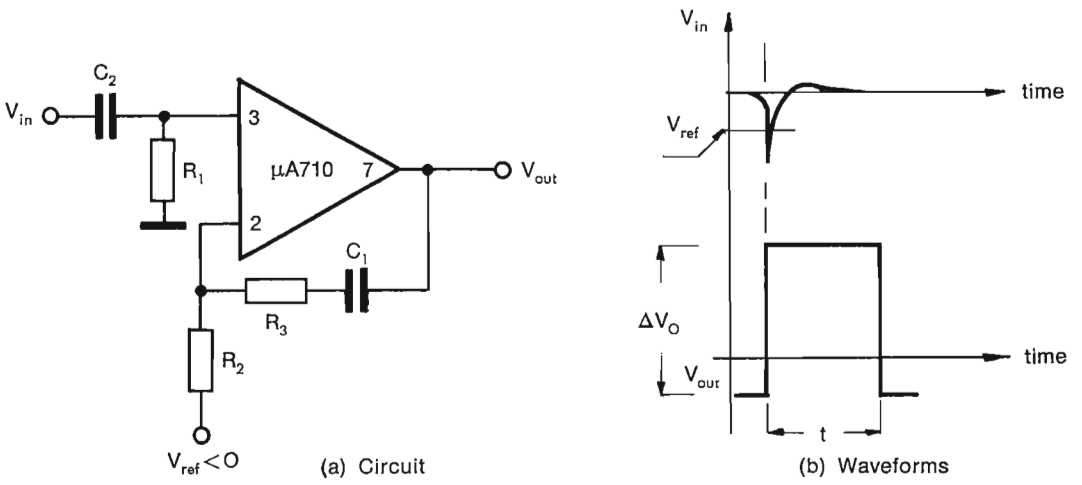


Fig. 3.48 - One Shot Mutivibrator

input pulse which exceeds V_{ref}. The output pulse is of constant amplitude with the duration which can be obtained from:

$$t = (R_2 + R_3)\, C_1 \log_e \frac{\Delta V_o R_2}{V_{ref}\,(R_2 + R_3)} \qquad \ldots\ldots\ldots (1)$$

or determined experimentally.

R_3 is used to reduce the recovery time (although it can be eliminated). It can be made 10 or 20 times larger than R_2 with a negligible loss in timing accuracy. It is also possible to obtain negative output pulses with a positive trigger pulse by making V_{ref} > zero.

Positive outputs for positive trigger pulses and negative outputs for negative pulses can also be obtained by connecting the trigger coupling capacitor (C_2) to the non-inverting input. However, the interaction between the trigger and feedback circuitry must be taken into account.

Note (1). Where stability of the triggering voltage point is important then R_1 and R_2 should be as low as practical, consistent with the other circuit requirements. The value of R_2 in series with the effective source resistance of V_{ref} should approximately equal the value of R_1.

Note (2). The value of ΔV_o is dependent mainly on the positive voltage supply and output load but would be typically + 3.7 V using supplies of + 12 V and — 6 V.

3.6.2 Free-Running Multivibrator

Fig. 3.49 shows a circuit configuration for a μA710 used as a fre-running multivibrator. The method of operation is as follows:

Positive feedback s applied via R_4 and R_3 to the non-inverting input. As the output, V_o changes from the « Low » to « High » state, the voltage level at pin (2) alters by an amount given by:

$$(V_{o\,max} - V_{o\,min})\,\frac{R_3}{R_3 + R_4} \qquad \ldots\ldots\ldots\ldots (1)$$

At the instant of switching, the voltage at the inverting input and hence at C_1 is equal to the original level of pin (2) in the « Low » state.

The capacitor now charges towards a voltage given by:

$$\frac{R_2}{R_1 + R_2}\left(V_{o\,max} + V^- \frac{R_1}{R_2}\right) \qquad \ldots\ldots (2)$$

Where V^- is the negative supply voltage amplitude and $V_{o\,max}$ is the voltage of the μA710 in the « High » state. The effective resistance for the time-constant would be:

$$R_{eff} \approx \frac{R_1 R_2}{R_1 + R_2}$$

The output remains « High » until the voltage at pin (3) reaches the level at pin (2) given by:

$$V_{pin(2)} = \frac{R_3}{R_3 + R_4} V_{o\,max} \qquad \ldots\ldots\ldots\ldots (3)$$

At this point the comparator changes state to the « Low » level and the above operation occurs in reverse.

Because of the fast response of the μA710, the multivibrator circuit can be operated to quite high frequencies. It has been used successfully to frequencies as high as 5 MHz.

At high frequencies, performance can be slightly improved by connecting a small capacitor between the output and the non inverting input.

Note (1). To ensure self-starting the μA710 is biased to give a D.C. operating point about the linear region. The ratio R_4:R_3 and R_1:R_2 are chosen such that the voltage which C_1 charges towards, given by equation (2), is always more positive than the voltage present at pin (2) when the output is at $V_{o\,max}$.

Note (2). For maximum stability of the operating point with temperature, the source impedance into pin (2) and (3) should be approximately equal.

Note (3). Using + 12 V and — 6 V typical values of + 3.2 V and — 0.5 V which correspond to output « High » and « Low » respectively, are obtained.

In such a condition the ratio R_4:R_3 and R_1:R_2 can be chosen such that the output square wave is symmetrical.

All these conditions can be satisfied if:

$R_2 = 9.7\ R_1$

$R_3 = 1.8\ R_1$

$R_4 = 1.8\ R_1$

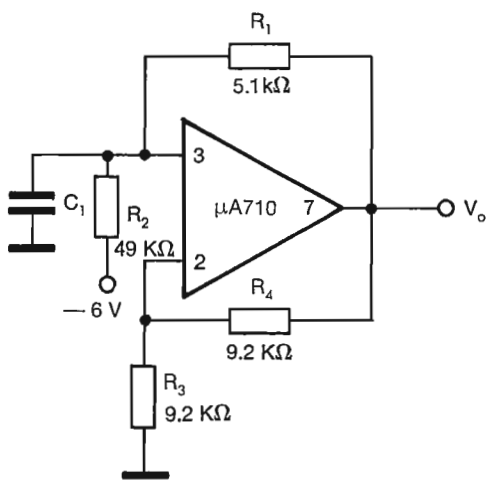


Fig. 3.49 - Free Running Multivibrator

There are certain restrictions, however, on the R_1 range.
If R_1 is smaller than about 1 kΩ the output sink current of the μA710 may not be large enough to swing the output all the way negatively.
On the other hand if R_1 is greater than about 24 kΩ, the input offset current could seriously effect the symmetry of the output waveform, thereby causing additional problems.

3.6.3 Core-memory Sense Amplifier

The circuit shown in Fig. 3.50 demonstrates an interesting application for the μA710. This is a core-memory sense amplifier (or threshold detector) which offers many advantages over conventional techniques.

Conventional sense amplifiers are usually differential-input, differential-output amplifiers which amplify the output of the cores and eliminate the large common-mode signals present during read-out. The actual sensing threshold is inserted in the output of the amplifier.

This system has the disadvantage that the offset voltage, the differential gain and the output common-mode level of the sense amplifier must all be accurately controlled, to get a precise threshold level. With

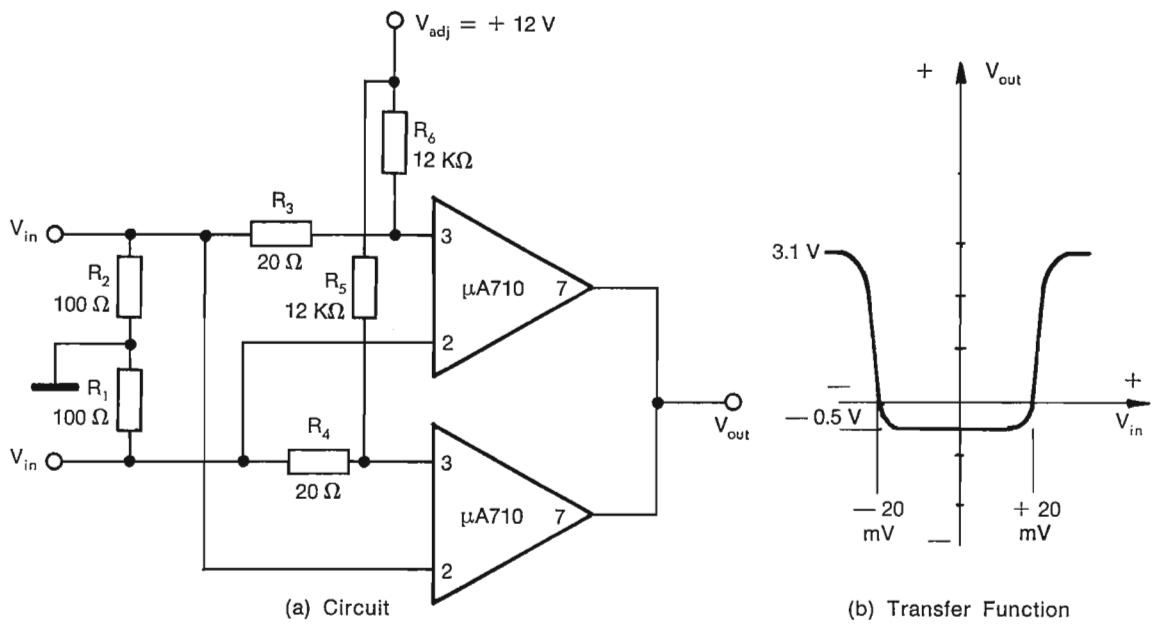


Fig. 3.50 - Core Memory Sense Amplifier

the circuit as shown, the threshold is inserted directly at the input so only the offset voltage of the comparator is important in determining the sense level. Since the offset is quite low in the μA710, the sense level can be accurately determined almost independent of temperature. In the circuit, R_1 and R_2, provide termination of the sense line. The sense level is essentially equal to the voltage across R_3 and R_4 caused by current from the positive supply (V_{adj}) through R_5 and R_6. Resistors R_1 and R_2 provide the return path to ground for this current. The sense level could be adjusted for each unit individually to take into account offset voltage by altering the value of R_5 and R_6. The sense level of a whole bank of circuits can be altered by variation of V_{adj}. A stable sense level within ± 5 mV may be obtained, however, using fixed circuit values and without voltage adjustment or selection of units.

The sense level will be affected by a common-mode signal, although only by approximately 8% for a 1 V signal if it is present during the read interval. This is seldom a problem because, in a typical memory store, the common-mode signal during read is less than 0.5 V.

The circuit is directly coupled and employs low storage-time devices. As a result, the recovery time from either differential or common-mode overloads is less than 50 nsec. The direct coupling also removes the pattern sensitivity of threshold voltage seen with A.C. - coupled amplifiers.

Input pulses of opposite polarity can be combined directly at the output, as shown, only for positive « ones ». Input pulses of opposite polarity can be separated if desired. When the outputs are separated, either positive or negative « ones » can be

obtained by switching the input terminals of the comparators.

No provision is made for strobing, since this can usually be accomplished with relative ease in the following logic circuitry. Even so, direct strobing can be done on the positive supply by driving it from a standy condition of + 7 V to + 12 V during the read interval. This has the additional advantage of reducing the standby power dissipation by a factor of 3.

In certain memories (i.e., biax) the sense line output is a pulse of one polarity for a stored zero and of the opposite polarity for a stored one. In these applications, only one μA710 is required for a sense amplifier. The differential input is connected directly across the sense line; during the strobe interval, the output will be in either a digital one or zero state depending on the input pulse polarity.

Note (1). A special integrated circuit package is available designated the μA711. This contains essentially two μA710 circuits together for use in applications such as described above. Reference should be made to the Section 2.9.

3.6.4 Crystal-Controlled Oscillator

Fig. 3.51 shows the circuit of a 1 MHz crystal-controlled oscillator. Positive feedback is provided from the output via the crystal to the non-inverting input.

The D.C. operating point is biased by means of R_1 and R_2 connected to the negative supply so that oscillation takes place about the linear (non-saturated) region, thus ensuring self-starting.

C_1 decouples R_2, removing negative feedback at the oscillation frequency. Resistor R_3, in addition to providing the load across which the positive feedback voltage is developed, also helps to stabilize the operating point with respect to temperature variations and should have the value,

$$R_3 \approx \frac{R_1 R_2}{R_1 + R_2}$$

Note (1). Using + 12 V and — 6 V supplies, the approximate mean output level is typically 1.35 V positive. If the non-inverting input is returned to ground via R_3 then the optimum bias point is determined from:

$$\frac{R_1}{R_2} = \frac{1.35}{V^-}$$ where V^- is the negative supply voltage,

and R_1 should not be greater than approximately 47 kΩ.

Note (2). In order to decouple the negative feedback to the inverting input, the value of C_1 is chosen so that at the oscillation frequency the reactance is given by:

$$X_C < \frac{R_1}{500}$$

With a suitable choice of component values, satifactory operation in excess of 5 MHz may be obtained with this circuit configuration.

3.6.5 Positive Peak Detector

One difficult problem that can be solved with the μA710 is the accurate measurement of the peak amplitude of very fast pulses. A peak detector which does this is shown in Fig. 3.52. The input signal is applied to the non-inverting input of the μA710. The

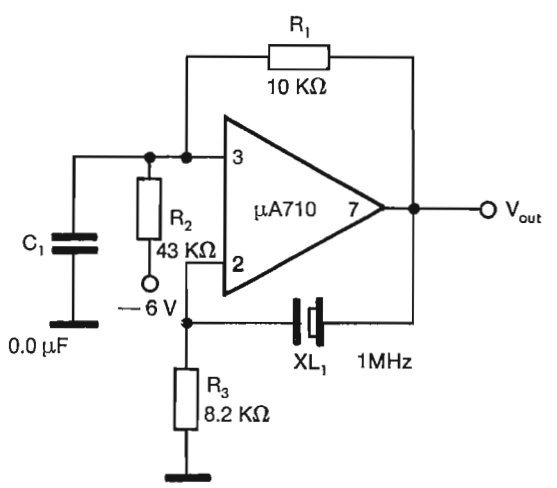
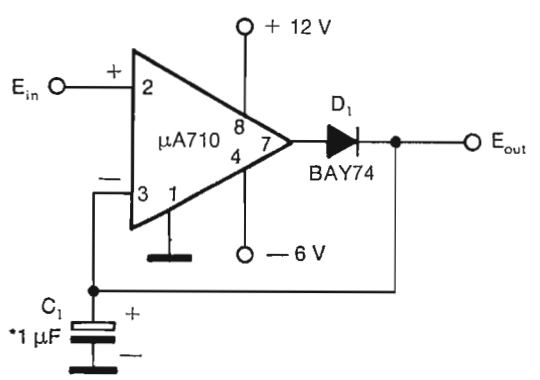


Fig. 3.51 - Crystal Controlled Oscillator



* Tantalum Slug Capacitor (Sprague Type 1500)

Fig. 3.52 - Positive Peak Detector for Fast Pulses

output is taken from a large capacitor connected to the inverting input. If the voltage on the input terminal is greater than that on the output, the comparator output will swing positive and charge the capacitor rapidly through D_1. When the input voltage drops below the voltage on the capacitor, the output of the μA710 swings negative and the diode becomes reverse-biased. This leaves the capacitor charged to the peak value of the input signal.

Because of the low offset and fast response time of the μA710, the circuit can measure the amplitude of a train of pulses less than 100 nsec duration with an accuracy of 5 mV. The operating range of the circuit, which is determined by the available output swing of the comparator, is 0 to + 2.5 V. The decay time of the voltage developed across the capacitor is determined by the input bias current of the μA710. This is approximately 20 msec/V. If it is desired that the peak detector follow more rapidly varying signals, a resistor can be inserted between the output and the negative supply voltage. The peak detector loads the signal source very little. The maximum current drawn from the source is approximately 25 μA, and this only occurs at the peak of the input signal.

The circuit functions as a unity-gain feedback amplifier at the peak of the input signal with C_1 providing frequency compensation. Hence, C_1 cannot be made much smaller than the 1 μF indicated or the circuit will oscillate at the peak of the input signal, giving erratic operation. However, larger values of capacitance can be used.

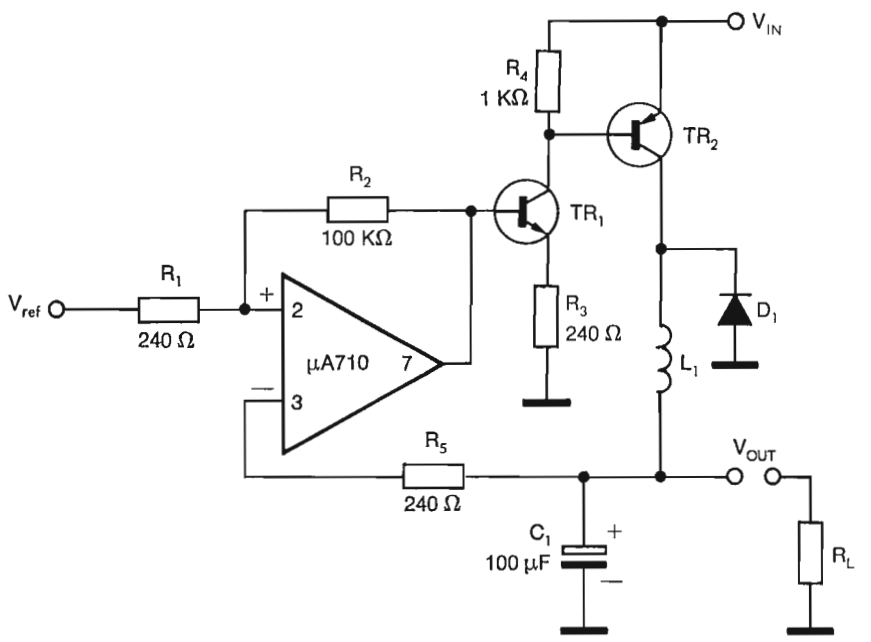


Fig. 3.53 (a) - Simplified Circuit of the Switching Regulator

3.6.6 High-Power Switching Regulator

Another circuit which demonstrates the flexibility of the μA710 is the high-power switching regulator shown in Fig. 3.53 (b). It is capable of delivering an output current greater than 2 A at better than 80% efficiency. The output voltage is adjustable over a very wide range, and the load and line regulation is better than 0.5%. The operating frequency is about 10 kHz and the output ripple is less than 10 mV. Current limiting, which keeps the dissipation in the power-switch transistor at a safe value, is provided.

The basic circuit can be explained with the aid of the simplified circuit given in Fig. 3.53 (a). The μA710 is connected as a level detector with hysteresis, and the regulator reference voltage is fed to the non-inverting input. Therefore, the comparator will switch on when the voltage on the inverting input is slightly below the reference; and it will switch off when this voltage is slightly above the reference. When the comparator turns on, it drives TR_1 which saturates TR_2, applying the D.C. input voltage to the load through L_1. The output voltage is sent back to the inverting input of the comparator; hence, when the

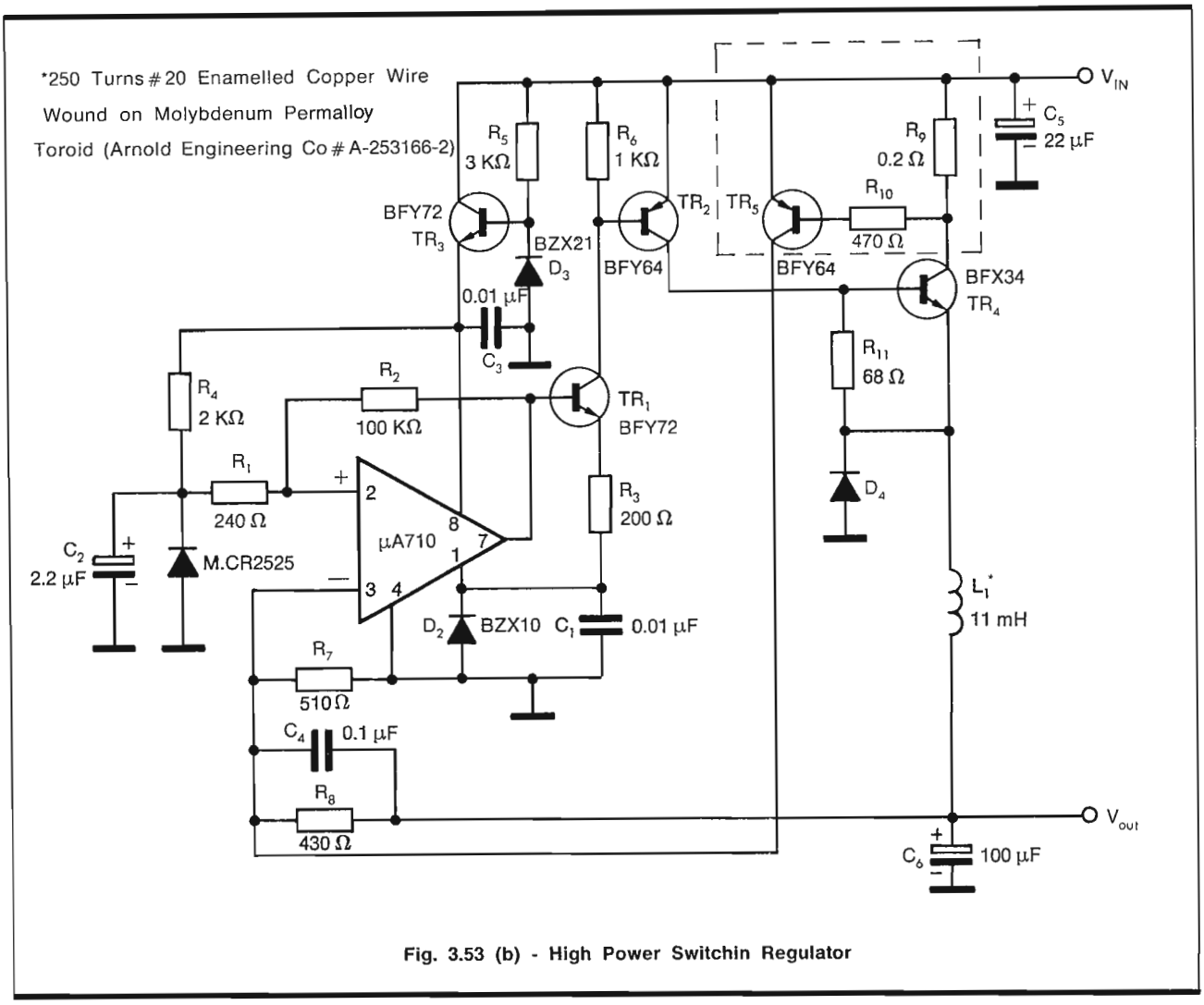


Fig. 3.53 (b) - High Power Switchin Regulator

output voltage rises above the reference voltage, the comparator turns off. The output voltage now falls at a rate determined by L_1 and C_1. When it drops by an amount equal to the hysteresis, the comparator turns back on; and the output again rises. Therefore, the circuit operates in a self-oscillating mode in such a way as to maintain a constant ripple voltage across the load independent of input voltage or load.

The purpose of the diode D_1 in Fig. 3.53 (a) is to provide a return path for the inductor current after the switching transistor turns off. The size of the inductor has a considerable influence on the efficiency. If the inductor is large enough to maintain a relatively constant current through the switching cycle, it is easy to see how it is supplying the load current continuously. However, this current (which is equal to the load current) is only being supplied by the input voltage source for part of the cycle. The inductor is acting as a source, supplying current through the diode, for the remainder. Therefore, the average input current is less than the output current. As the inductor is made smaller, the peak currents become greater, increasing the losses in the power switch transistor, the inductor, and the diode.

An interesting feature of the circuit is that if the inductor is made large enough so the current through it does not go to zero through the cycle, the operating frequency will be affected little by the load or the input voltage. Instead, it will be determined by the inductor, the output capacitor, and the amount of hysteresis on the comparator.

The complete circuit of the switching regulator is shown in Fig. 3.53 (b). A pre-regulator (TR_3, R_5 and D_3) is used to supply current for the temperature-compensated, voltage-reference diode, D_1. The pre-regulator also provides power for the µA710. The comparator is operated from supply voltages of 0 V, + 6 V, and + 18 V instead of the usual positive-negative voltage combination. The + 6 V is provided by zener diode, D_2. An emitter-follower transistor, TR_4, is added at the output to increase the output-current capability. TR_5 serves as the current-limiting transistor: when the peak output current exceeds about 3 A, the power switch transistor is no longer required to maintain the output voltage. Instead, TR_5

supplies current directly to the inverting input of the comparator. Therefore, the power transistor still switches and does not have to handle anywhere near the full short-circuit current at the maximum supply voltage as would be required with conventional current-limit schemes.

The output voltage is established with the resistive divider formed by R_7 and R_8. A potentiometer can be substituted to make this voltage continuously variable with the zener reference voltage determining the lower limit of adjustment and the input voltage and breakdown voltage of the discrete transistors determining the upper limit. If additional ripple filtering is desired, it can be added without degrading regulation by connecting R_8 to the output of the added filter instead of to C_6, keeping C_4 connected to C_6 to provide the self-oscillating feedback. Resistor R_8 can also be used for remote-voltage sensing in this manner.

Because of the relatively high operating frequency of the circuit, all large value capacitors should be solid tantalum and all the low-value capacitors should be disc ceramic in order to provide adequate bypassing.

3.7 μA711 BASIC CIRCUITS

3.7.1 Sense Amplifier Circuits

Conventional sense amplifiers are usually differential-input, differential-output amplifiers which amplify the output of the cores and eliminate the comparatively large common-mode signals present during read. A full- wave rectifier and sense-level threshold are inserted at the output of the amplifier to discriminate between the zero and one outputs of the cores.

This approach has the disadvantage that the offset voltage, the differential gain, the output common-mode level, the rectifier offset, and the output threshold level must all be accurately controlled to get a precise input-referred threshold level. A much more satisfactory solution is to use a voltage comparator and insert the threshold voltage at the input.

In this case, the accuracy is only affected by the offset voltage of the comparator (which similarly affects the differential amplifier in the conventional approach).

Variations in voltage gain and frequency response do not affect accuracy as long as these are high enough.

The problem in using a voltage comparator as a sense amplifier has been that the threshold voltage is not easily inserted at the input when common-mode rejection is required. A straightforward approach to the problem requires a floating voltage source. However, the circuit in Fig. 3.54 (a) inserts the threshold at the input using a grounded supply, yet it provides respectable common-mode rejection. In the circuit, R_1 and R_2 provide termination for the sense line. The sense level is essentially equal to the voltage across R_3 and R_4 caused by the current from the positive supply (V_{adj}) through R_5 and R_6. The grounded tap on the line termination resistors provides a sink for this current. The use of two comparators enables the circuit to responde to either positive or negative input signals above the preset threshold.

The advantages of this approach using the dual comparator are many. It does not require anything that is difficult to do in the integrated circuit, which

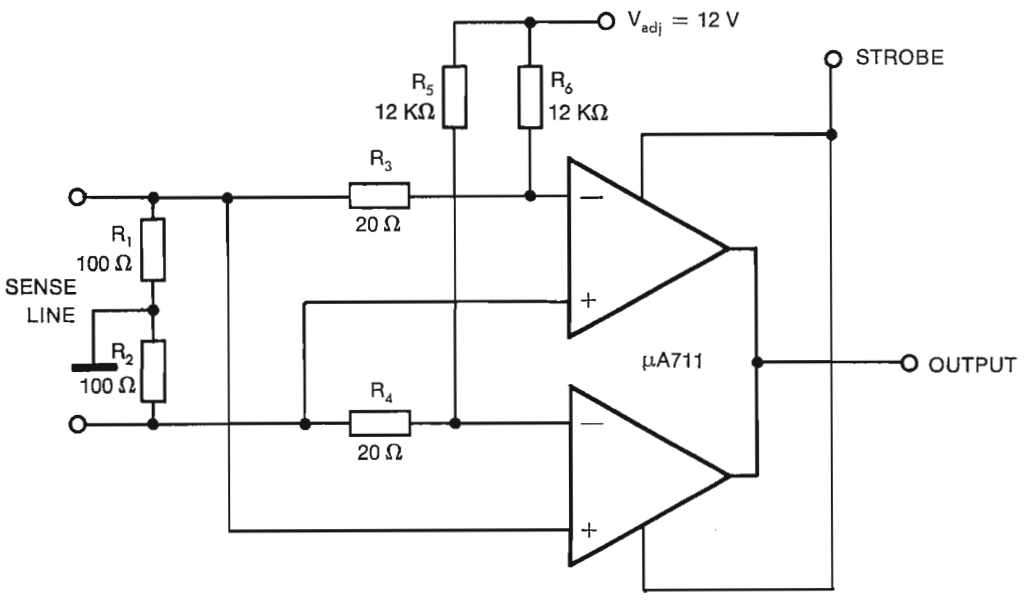


Fig. 3.54 (a) - Basic Sense Amplifier Configuration

means that it can be produced and delivered. Further, the threshold level is determined by inexpensive external resistors so a single dual comparator design can be used for a wide variety of core sizes. This permits standardization and allows production volumes that make use of the true economies of integrated circuits. The threshold voltage can also be easily adjusted to match the optimum value for a particular memory bank. This is done with a single adjustment for the entire battery of sense amplifiers by varying V_{adj}. In addition, because only input offset voltage is the prime determinant of threshold inaccuracy, the change of threshold voltage with temperature can be held to a minimum. This is important even though core outputs vary substantially with ambient temperature for a constant current drive. The reason is that if write and read functions are to be done at different temperatures, the core variation must be compensated with the current drive for the cores. If an attempt is made to compensate for core thermal variations with corresponding thermal changes in sense amplifier threshold, it is not practical to write into the cores at one temperature and read out at another. The best situation is for the sense amplifier to maintain a constant threshold over the full temperature range.

With the circuit in Fig. 3.54 (a) the sense level will be affected by a common-mode signal, although only by approximately 8 percent for a one-volt signal with $V_{adj} = 12$ V. This is rarely a problem because the common-mode signal during read is less than 0.5 V in most memories. This sensitivity can be reduced by increasing R_5 and R_6 and using a higher voltage to set the threshold.

Because the comparator is directly coupled and employs low storage time devices, the recovery from either differential or common-mode overloads is less than 50 ns regardless of their amplitude. The direct

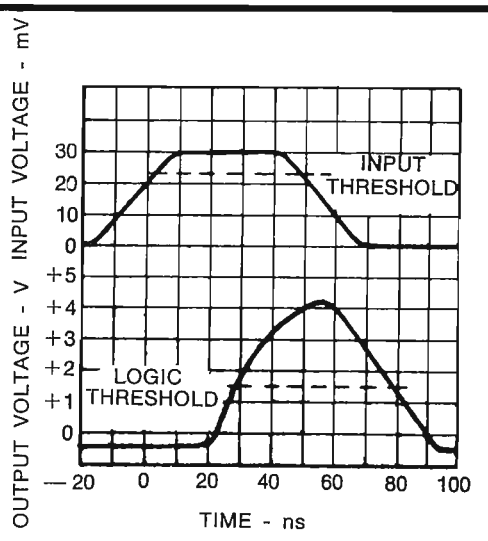


Fig. 3.54 (b) - Response of the Basic Sense Amplifier Circuit, with a 23 mV Threshold Setting to a 30 mV Input Pulse

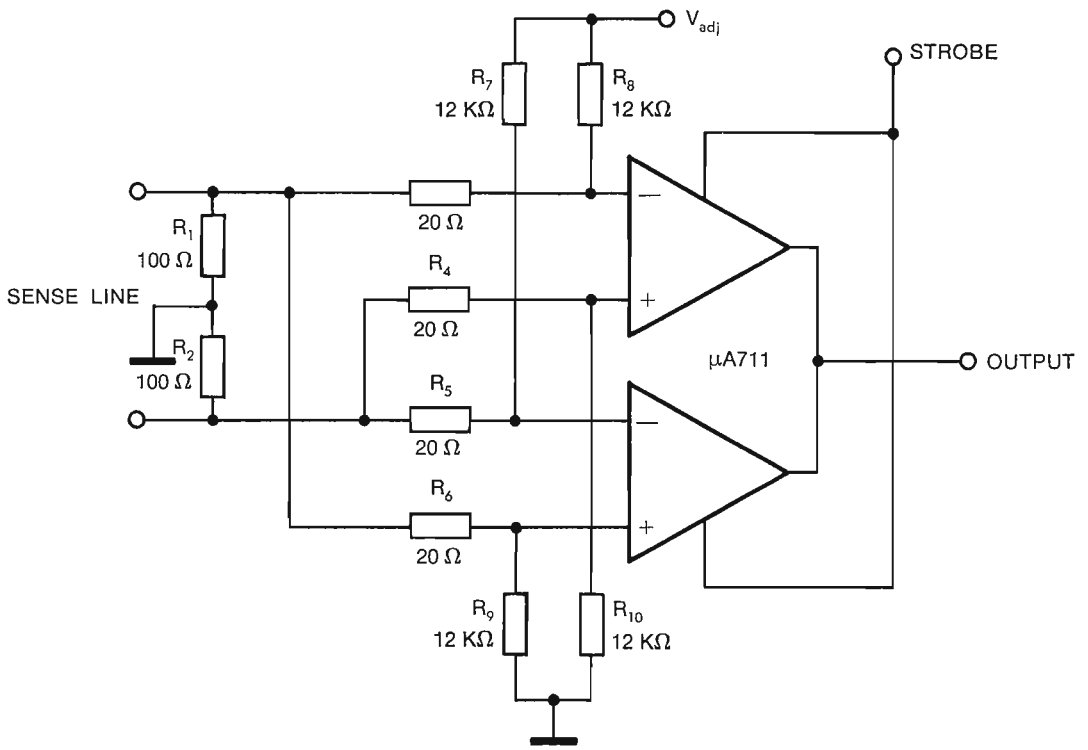


Fig. 3.55 - Sense Amplifier with Improved Insensitivity to Common Mode Signals

coupling also removes the pattern sensitivity of threshold voltage seen with A.C. - coupled amplifiers.

The response of the sense amplifier to a typical input one is shown in Fig. 3.54 (b). With an input signal that is 7 mV above the discrimination level for 45 ns, an output pulse that is above the logic threshold for 50 ns is obtained. Longer output can be obtained using the pulse stretching techniques described in Section 2.10.1.

3.7.2 Sense Amplifier with Improved Insensitivity to Common-mode Signals

In the unusual case where very large common-mode signals are present during read, the circuit in Fig. 3.55 can be used. This circuit uses additional resistors to balance the input bias network to the common-mode signal, and it provides a common-mode rejection of at least an order of magnitude better. This circuit is especially useful if the resistor network is purchased as a thin (or thick) film assembly since the extra resistors add little complexity to the complete assembly and since the tolerance on the balancing resistors can be looser than the tolerance on the threshold-determining resistors.

The high-frequency common-mode rejection can be severely degraded by unbalanced stray capacitances on the sense line and on the comparator input. For this reason, low-capacitance resistors should be used for R_5, R_6, R_3 and R_4, the physical layout should also be such as to minimise strays.

3.7.3 Sense Amplifier Circuit Using Temperature-compensated Preamplifier

When working with very small cores, the output signal can be so small as to approach the offset of the comparator. In this case, some sort of amplification is required before going into the sense amplifier. In addition, since D.C. offset will be a basic limitation on discrimination level in the preamplifier stage, A.C. coupling is also required. A method of accomplishing this is shown in Fig. 3.56 (a). A differential input stage is used as a preamplifier with a gain of 10. Its output is coupled into the dual comparator connected as a sense amplifier, with a threshold voltage setting of 50 mV, in a circuit similar to that in Fig. 3.54 (a). An inductor (L_1) is used to remove the offset of the input stage transistors so a matched pair does not have to be

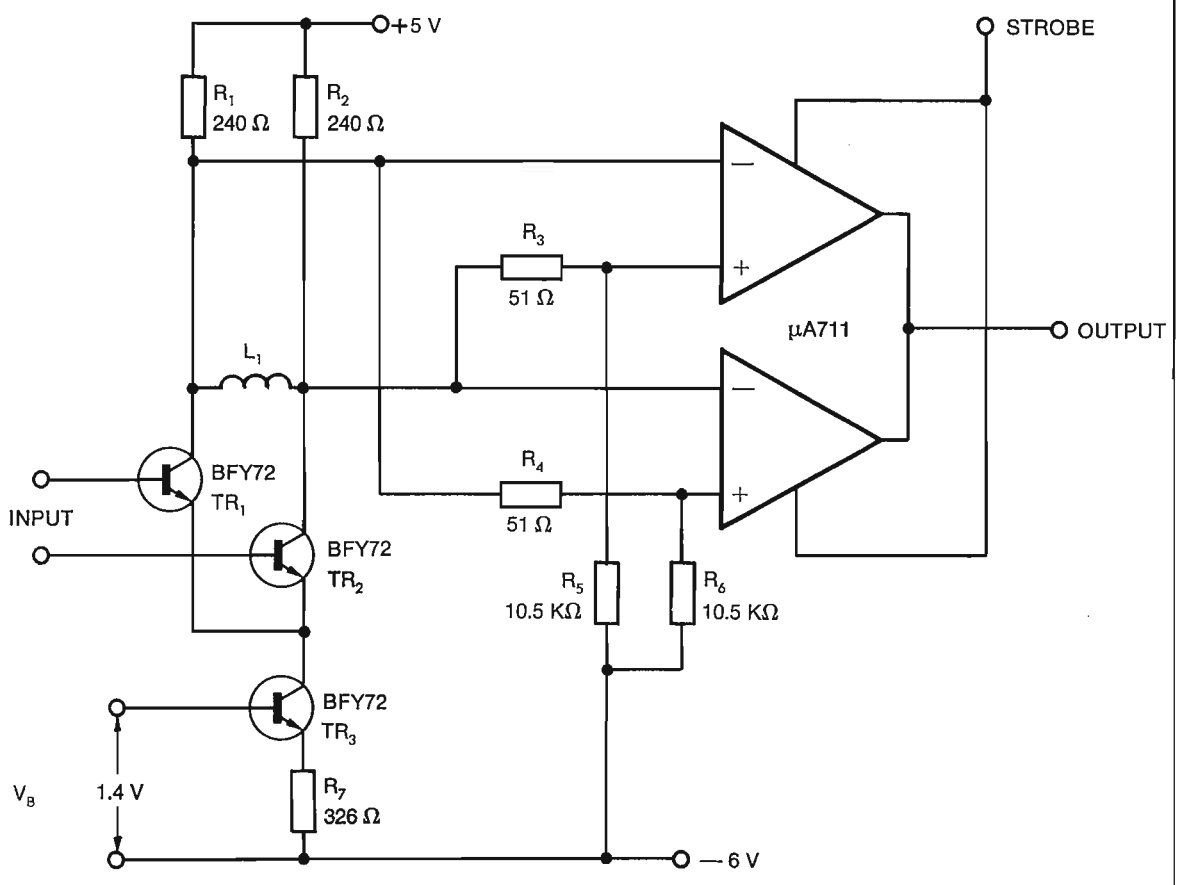


Fig. 3.56 (a) - Sense Amplifier Circuit Using Temperature Compensated Preamplifier for Increased Threshold Sensitivity

used. The differential preamplifier achieves temperature compensated operation, within a few percent, over the entire —55°C to +125°C temperature range without the use of emitter degeneration resistors. This is an advantage since the degeneration resistors deteriorate common-mode rejection and give non-optimum high-frequency characteristics. The voltage gain of the differential preamplifier is made insensitive to temperature by choosing a suitable bias voltage, V_B, for TR_3. The optimum bias voltage was empirically determined to be 1.4 V for —55°C to + 125°C operation. This gives a gain stability of ± 5 percent over the full temperature range for all units with a room temperature h_{FE} greater than 50. For limited temperature range operation (0-70°C), the optimum bias voltage is 1.3 V, and a 1% gain stability can be realized.

The gain of the preamplifier, and therefore the equivalent input referred threshold voltage, is most conveniently set by adjusting R_7.

With the circuit as shown in Fig. 3.56 (a), the sense threshold is 5 mV. Both the input stage and the dual comparator circuit provide common-mode rejection. The response of the sense amplifier to a 10 mV input signal is shown in Fig. 3.56 (b), this can be improved by operating the preamplifier stage at a higher current than the nominal 1 mA in the indicated design.

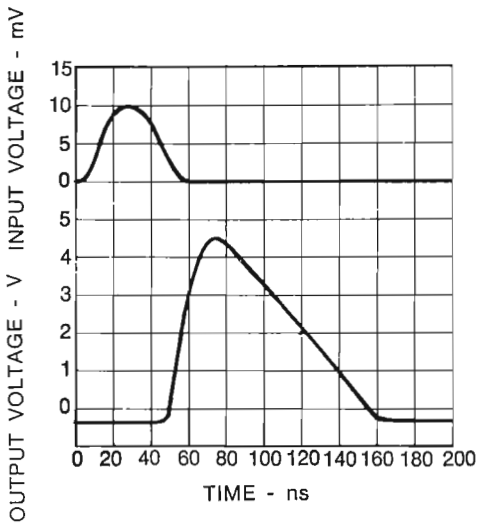


Fig. 3.56 (b) - Response to 10 mV input Pulse for 5 mV Threshold

3.7.4 Dual Sense Amplifier for Positive-on, Negative-zero Memory Systems

Certain types of memories (i.e., biax or non-destructive read) give an output of one polarity for a one and an output of the opposite polarity for a zero. In these applications, one-half the μA711 can be used as a sense amplifier. No resistor network need be employed on the input to determine threshold since the comparator alone is designed to detect zero crossing. The complete μA711 can be used as a dual-sense amplifier with common outputs. The outputs can be separated as far as the system logic is concerned by using the independent strobe terminals. A circuit for this is shown in Fig. 3.57.

3.7.5 Double-ended Limit Detector

The μA711 dual comparator was designed primarily for core-memory sense amplifier applications. However, it is sufficiently versatile to be used in a

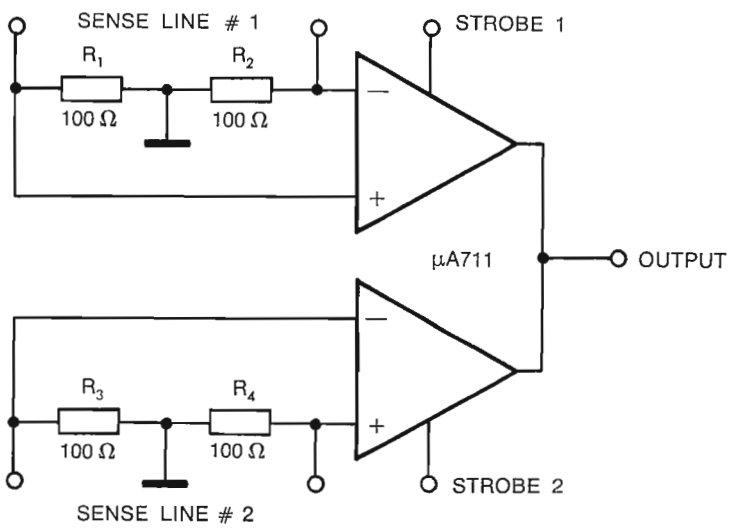


Fig. 3.57 - Dual Sense Amplifier for Positive-one, Negative-zero Memory Systems

number of other applications. One of these is shown in Fig. 3.58. The circuit gives a positive output for input signals below a preset threshold or above a second, independently adjustable voltage threshold. This output is fed to a lamp driver; hence, whenever the input signal goes outside the tolerance limits, the lamp will light. A feature of the circuit is that the limit detector can be disabled when it is not being used by applying a zero logic signal to the strobe terminals. In addition, up to eight dual comparators can be wired with common outputs and be used to feed a single lamp driver.

Details of the design are that the relative values of the source resistances for the signal and reference voltages should be as indicated in the circuit to make the accuracy dependent only on offset currents rather than bias currents. Ideally, these resistances should be as low as possible. The lamp driver design is such that its peak output current is limited during the initial turn-on of the bulb when the filament resistance is low. This is accomplished with R_2. Series resistor R_1 limits the output current of the comparator when the lamp driver saturates.

3.7.6 Double-ended Differential Threshold Detector with Hysteresis

Fig. 3.59 shows a double-ended differential threshold detector. In this circuit hysteresis is provided at both the upper and lower threshold levels. A μA709 operational amplifier serves as both a buffer and a difference amplifier. With component values shown, an output is obtained from the μA711 when the difference between the two input voltages exceed 0.55 V. A hysteresis of approximately 50 mV is obtained.

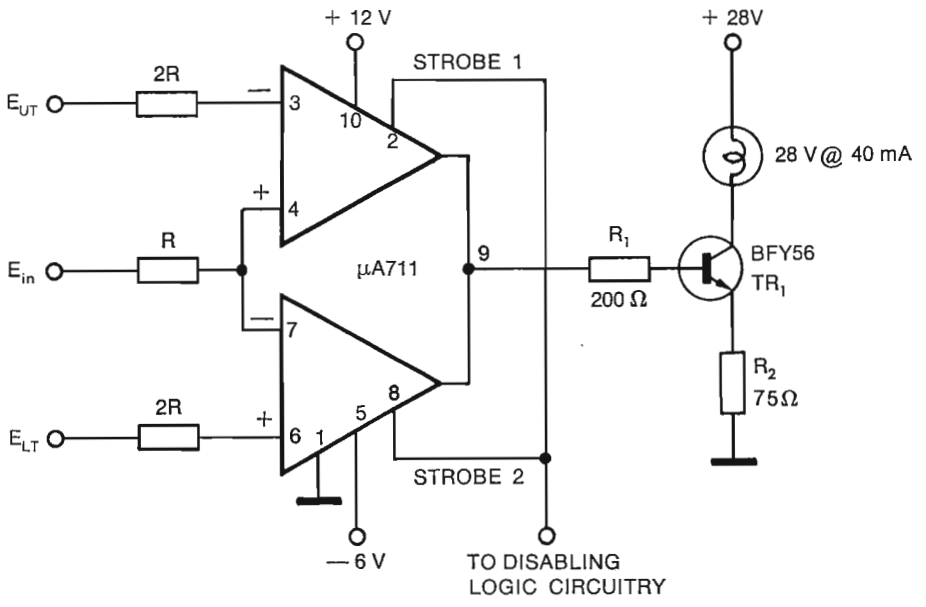


Fig. 3.58 - Double-ended Limit Detector for Automatic Go No-go Test Equipment

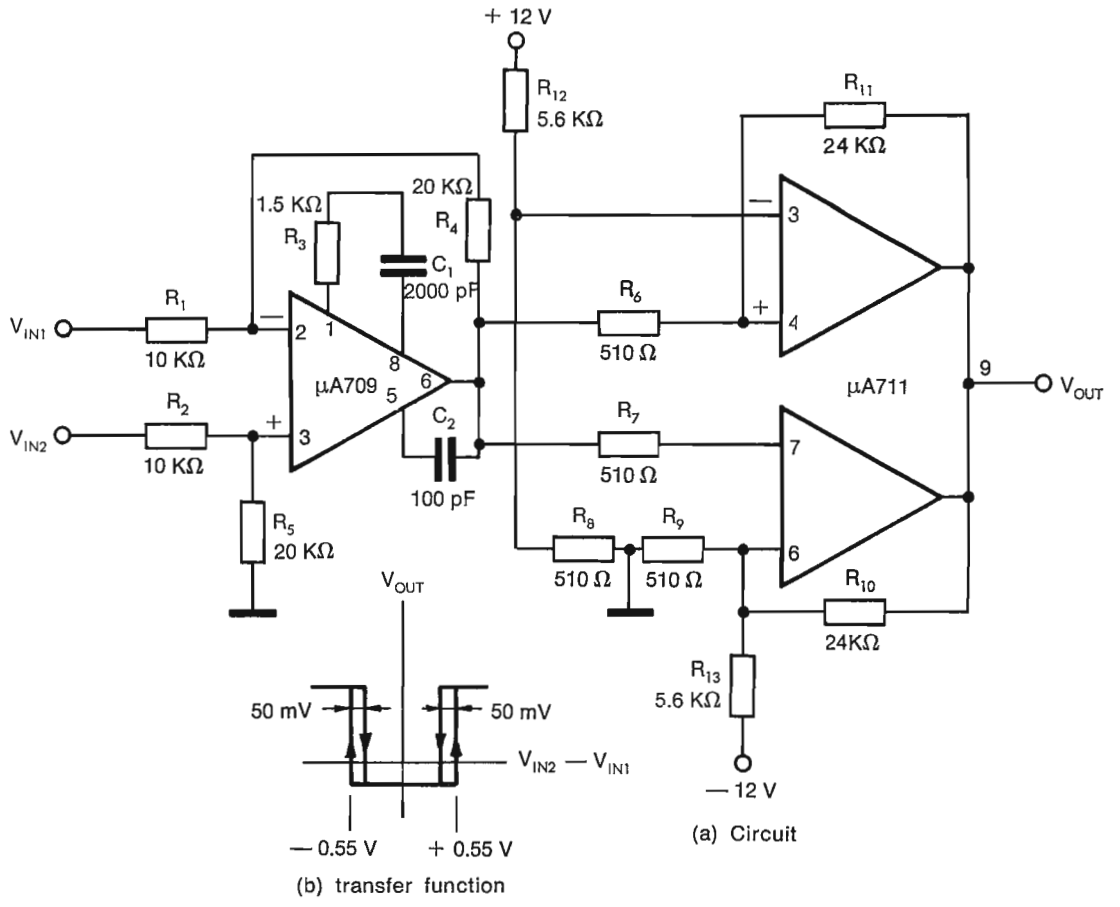


Fig. 3.59 - Double-ended Differential Threshold Detector with Hysteresis

4. MEASUREMENT OF INTEGRATED CIRCUIT BASIC PARAMETERS

4.1 INTRODUCTION

This Section describes fairly simple test circuits which may be used either to investigate in greater detail certain integrated circuit parameters, for example, the effects of variation in temperature or power supply voltage on offset current, open loop gain, etc., or merely to check that a suspected device is still functional and conforms to specification.

In order that better use may be made of the circuits described, it is strongly recommended that the other Sections of this Handbook are read first, in particular Section 5 on Frequency Compensation and Section 7 on Power Supplies.

4.2 TEST CIRCUITS

4.2.1 General Functional Test

The measure of large signal gain, linearity and output voltage swing can be found from the amplifier open-loop transfer function, which is a display of the input/output characteristics of the circuit over its full dynamic range.

The transfer function is obtained by applying the A.C. input and output signals of the device under test to the horizontal and vertical inputs of the oscilloscope, respectively.

The resultant oscilloscope trace is a plot of the amplifier output versus input: maximum output voltage swing, linearity and gain can be determined from the curve shown in Fig. 4.1.

The basic circuits for different devices are shown in Fig. 4.2.

D.C. stabilization of the operating point for the amplifier must be provided: this is because the D.C. gain is very high and an offset of few millivolts is enough to hold the output in saturation over part or all of the input cycle.

The amplifier is effectively tested under open-loop conditions, since at frequencies above 1 kHz the reactance of C_2 is negligible when compared to R_4.

Both C_1 and C_2 should be of low leakage type and capable of efficient operation at high frequencies.

Solid tantalum or ceramic types are suitable.

The A.C. signal for the transfer fuction is applied to the input of the Device under test through a precision attentuator (R_1, R_2).

The need for a high-gain horizontal deflection amplifier is eliminated by connecting the horizontal input of the oscilloscope to the high-level terminal of the divider.

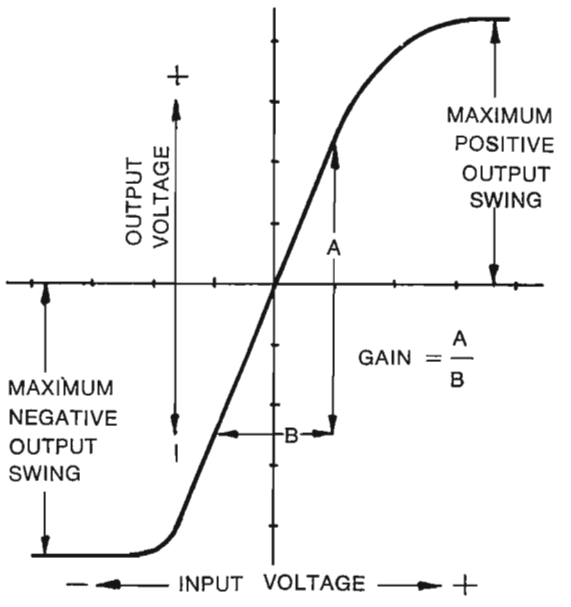


Fig. 4.1 - Transfer Function Display

4.2.2 Common-mode Rejection Ratio and Input Voltage Range

The common-mode rejection ratio is defined as the ratio of the input voltage range to the maximum change in input offset voltage over this range, and the input voltage range as the range of voltage on the input terminals for which the device will operate within specifications.

Fig. 4.3 (a) and (b) show circuits suitable for measuring the above-mentioned parameter for the μA702 and μA709.

Resistors R_2, R_3 and R_1, R_4 set the amplifier voltage gain A_f to 100 and provide the D.C. current path to the input.

These resistances must be closely matched otherwise different tolerances will affect the test.

For the μA702A the input signal change between + 0.5 and — 4 V (which is the minimum guaranteed input voltage range) and the common-mode rejection ratio (CMRR) is given by:

$$\text{CMRR} = \frac{A_f V_{in}}{\Delta V_{out}} = \frac{450}{\Delta V_{out}}$$

This is usual to express this ratio in dB and therefore this formula would be given by:

$$\text{CMRR} = 20 \log \frac{450}{\Delta V_{out}}$$

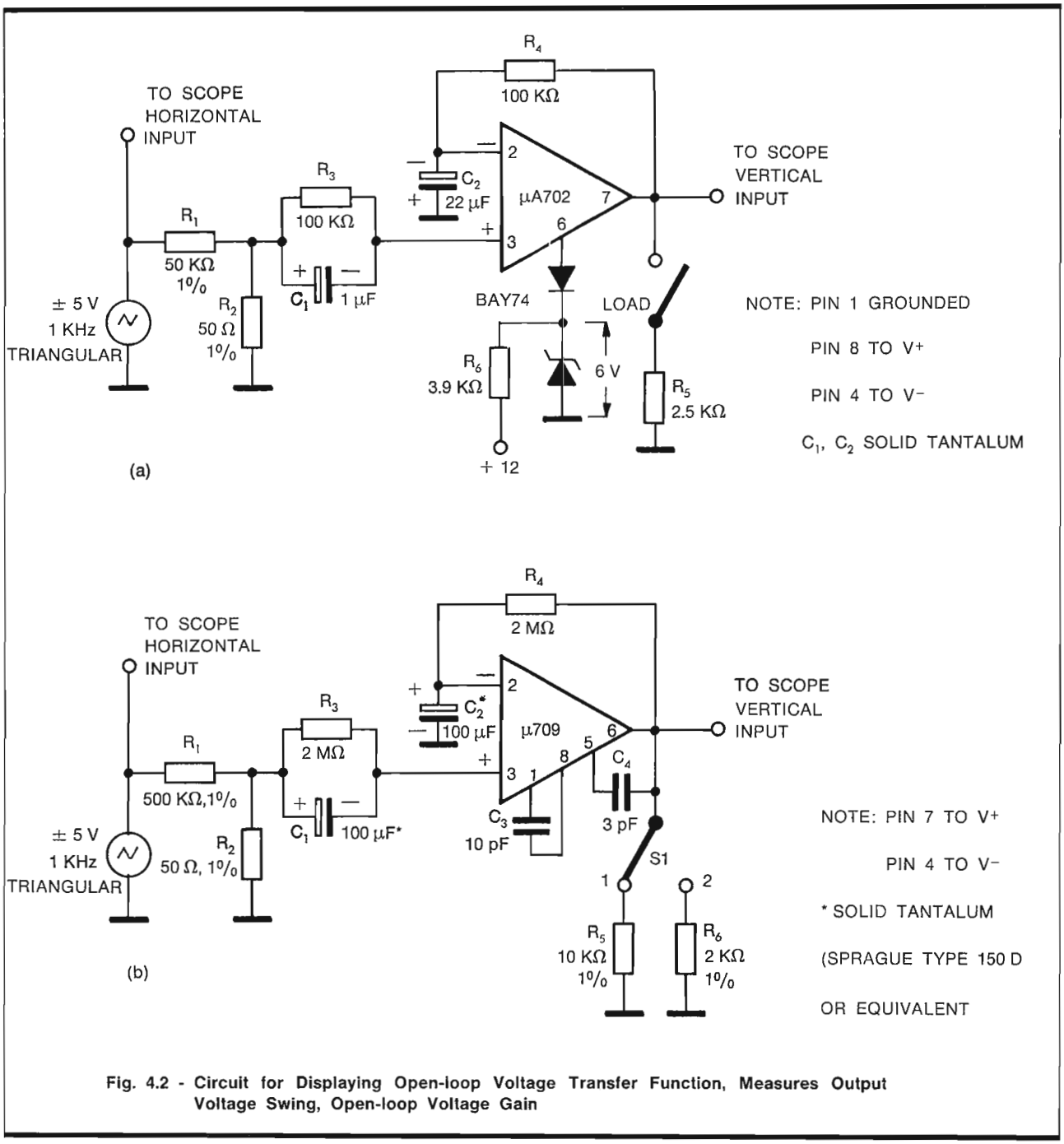


Fig. 4.2 - Circuit for Displaying Open-loop Voltage Transfer Function, Measures Output Voltage Swing, Open-loop Voltage Gain

Obviously for supply voltages lower than + 12 V and — 6 V proportionally less signal amplitude should be used.

For the µA709 the input voltage range is symmetrical (± 8 V).

Therefore the CMRR is given by:

$$\frac{1600}{\Delta V_{out}}$$

or

$$20 \log \frac{1600}{\Delta V_{out}}$$

For a supply voltage lower than ± 15 V proportionally less signal amplitude should be used.

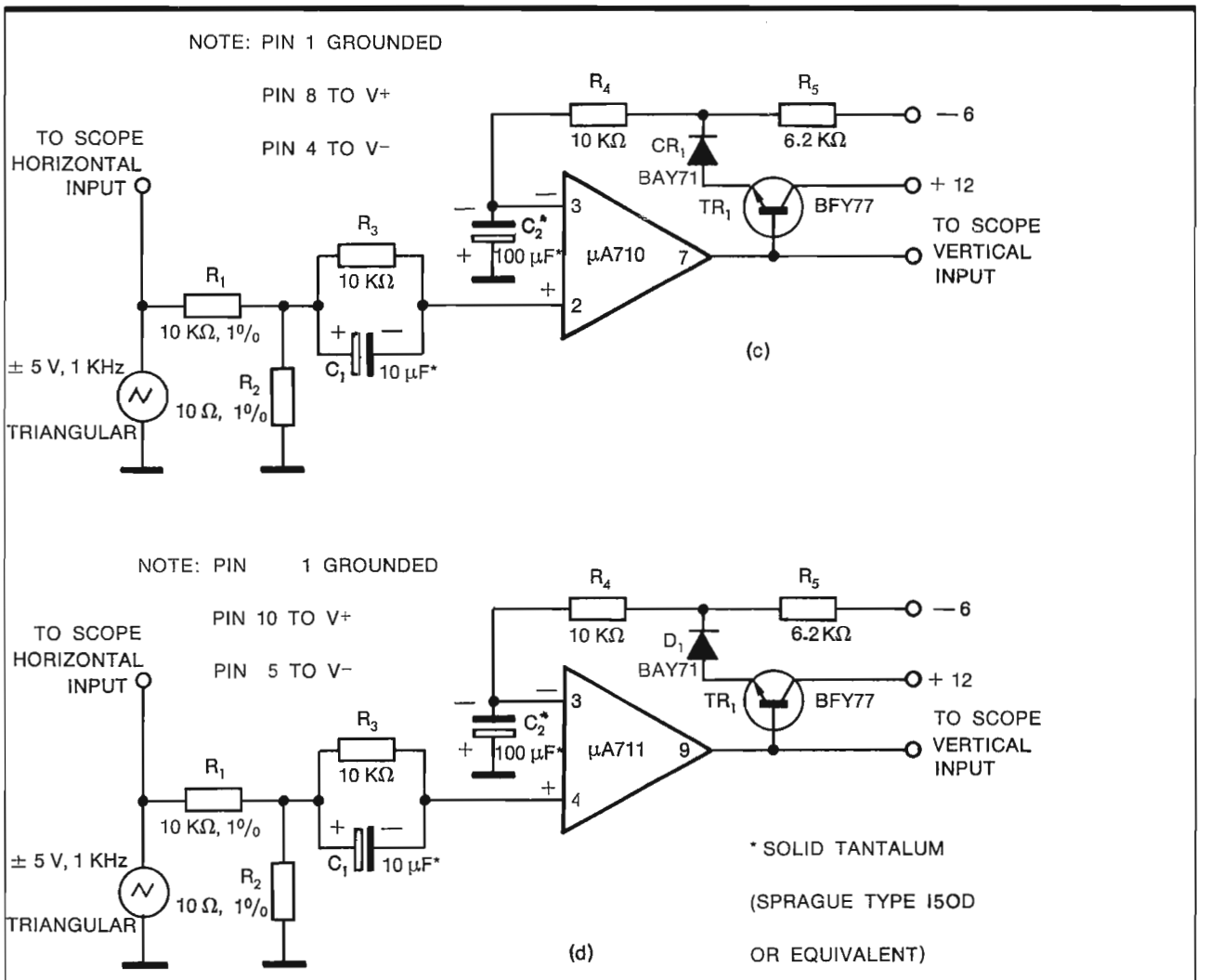


Fig. 4.2 - Circuit for Displaying Open-loop Voltage Transfer Function, Measures Output Voltage Swing, Open-loop Voltage Gain

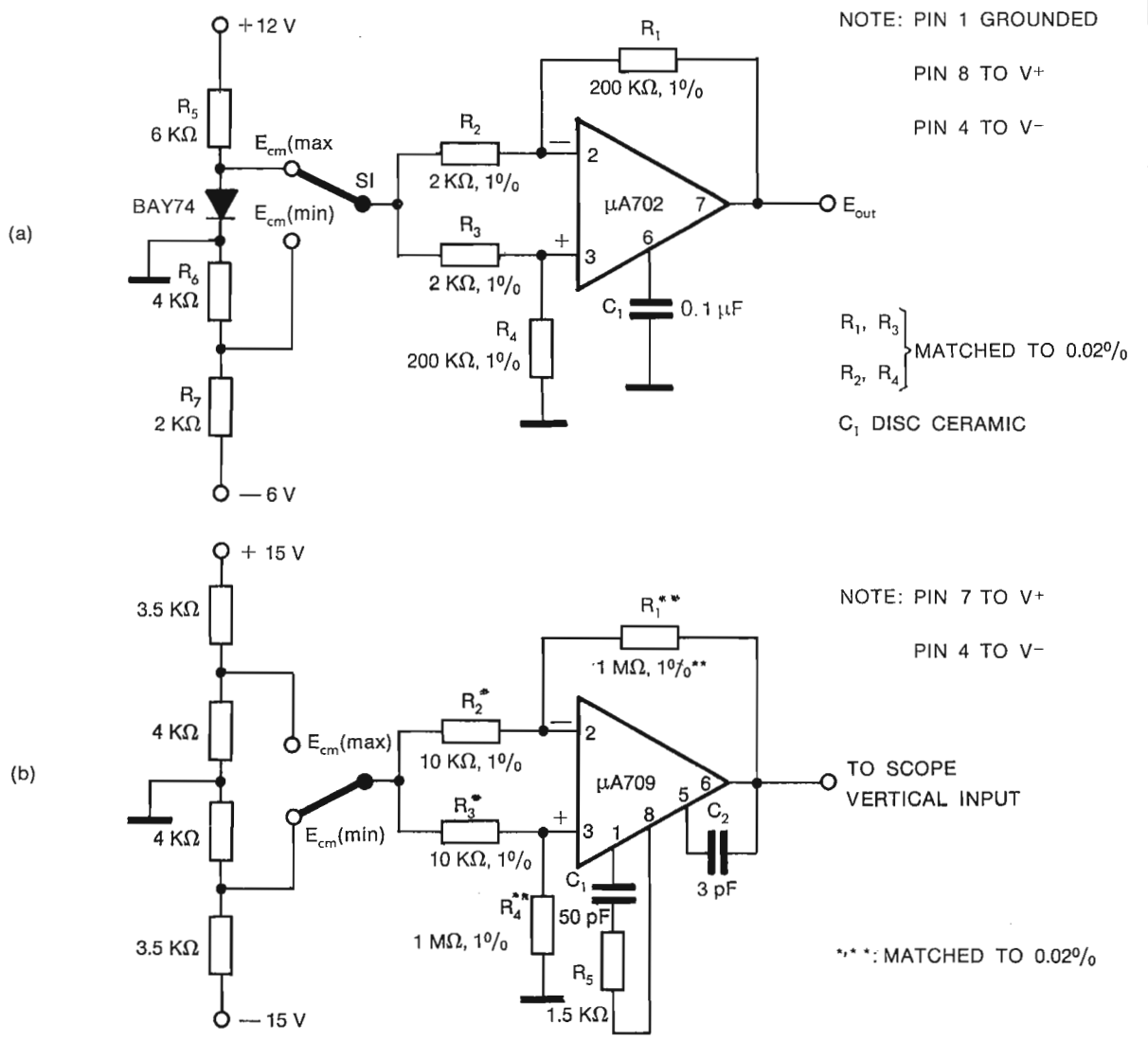


Fig. 4.3 - Circuit for Measuring Input Common Mode Rejection Ratio and Input Voltage Range

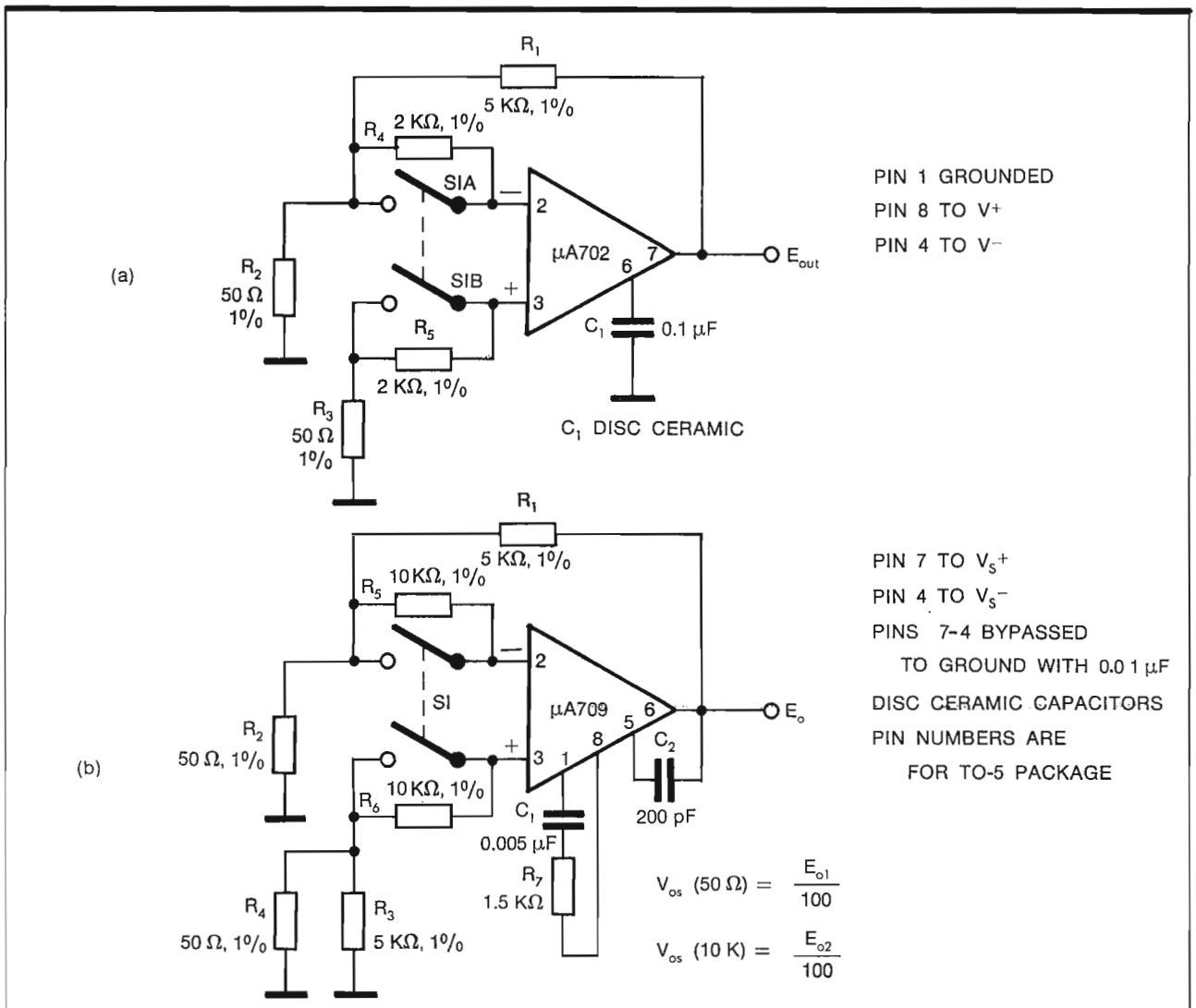


Fig. 4.4 - Circuit for Measuring Input Offset Voltage and Power Supply Sensitivity

4.2.3 Input Offset Voltage

The input offset voltage is defined as the voltage which must be applied between the input terminals to obtain zero output voltage (μA702A and μA709) or a logic threshold voltage (μA710 and μA711).

The input offset voltage may also be defined for the case where two equal resistors are connected in series with the input leads.

Fig. 4.4 (a) and (b) show the circuits to measure this parameter for the μA702A and μA709. For good sensitivity it is preferable to make R_1 at least 100 times greater than R_2, so that the oscilloscope or digital voltmeter used to read the output will be able to operate on a convenient range.

Resistor R_2 should be kept at the lowest feasible value to prevent current offset from superimposing its effect on the voltage offset measurements, 50 Ω is a suitable value.

The input offset voltage is obtained by

$$V_{offset} = \frac{V_{out}}{100}$$

With S_1 open, the effective source resistance is increased by 2 kΩ for the μA702A and by 10 kΩ for the μA709.

Fig. 4.4 (c) and (b) show the circuits used to determine the input voltage offset of the μA710 and μA711.

The procedure is simple: obtain the logic voltage threshold at the output, adjusting V_{AD} and read this voltage.

The input offset voltage is given by:

$$V_{offset} = V_{AD}\frac{R_3}{R_3+R_4} = \frac{V_{AD}}{1000}$$

Therefore the value of V_{AD} expressed in volts gives the input voltage offset in millivolts.

Finally, with S_1 open the effective source resistance is increased to 200 Ω.

For the μA711 the measurements must be repeated for each side, with the other side disabled and with the strobe terminal connected to ground.

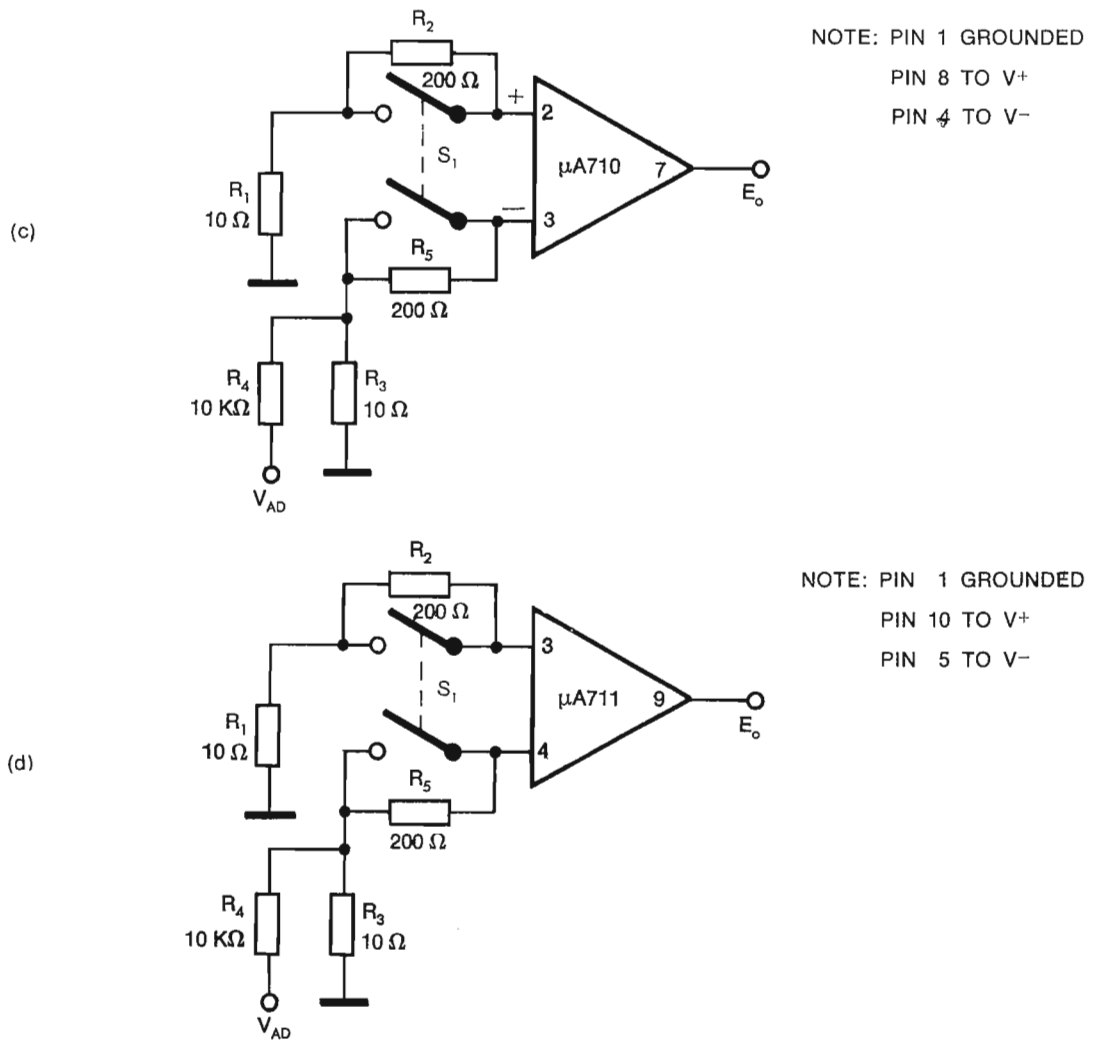


Fig. 4.4 - Circuit for Measuring Input Offset Voltage and Power Supply Sensitivity

4.2.4 Input Offset Current

Input offset current is the difference between the currents into the two input terminals with the output at zero voltage (μA702A and μA709) or at the logic threshold voltage (μA710 and μA711).

Fig. 4.5 (a) and (b) show circuits to measure the input offset current for μA702A and μA709.

The D.C. output voltage is given by:

$$V_{OUT} = I_{offset} R_2 + V_{offset}$$

Obviously the source resistance $R_2 = R_1$ is chosen so that the term $I_{offset} R_2$ is greater than the voltage offset: in such a condition the above-mentioned relation becomes:

$$I_{offset} = \frac{V_{OUT}}{R_2}$$

The capacitors C_1 and C_2 should be of the very low leakage type and capable of efficient operation at high frequencies.

Fig. 4.5 (c) and (d) show circuits suitable to determine the current offset for the μA710 and μA711.

The procedure is very simple: V_A has to be adjusted until the output level reaches the logic threshold. The input offset current is given by

$$I_{offset} = \frac{V_A}{R_2}$$ since R_2 has been chosen so that the influence of the offset voltage is negligible.

For the μA711 the test must be repeated for each side, with the other one disabled, and connecting the strobe lead to ground.

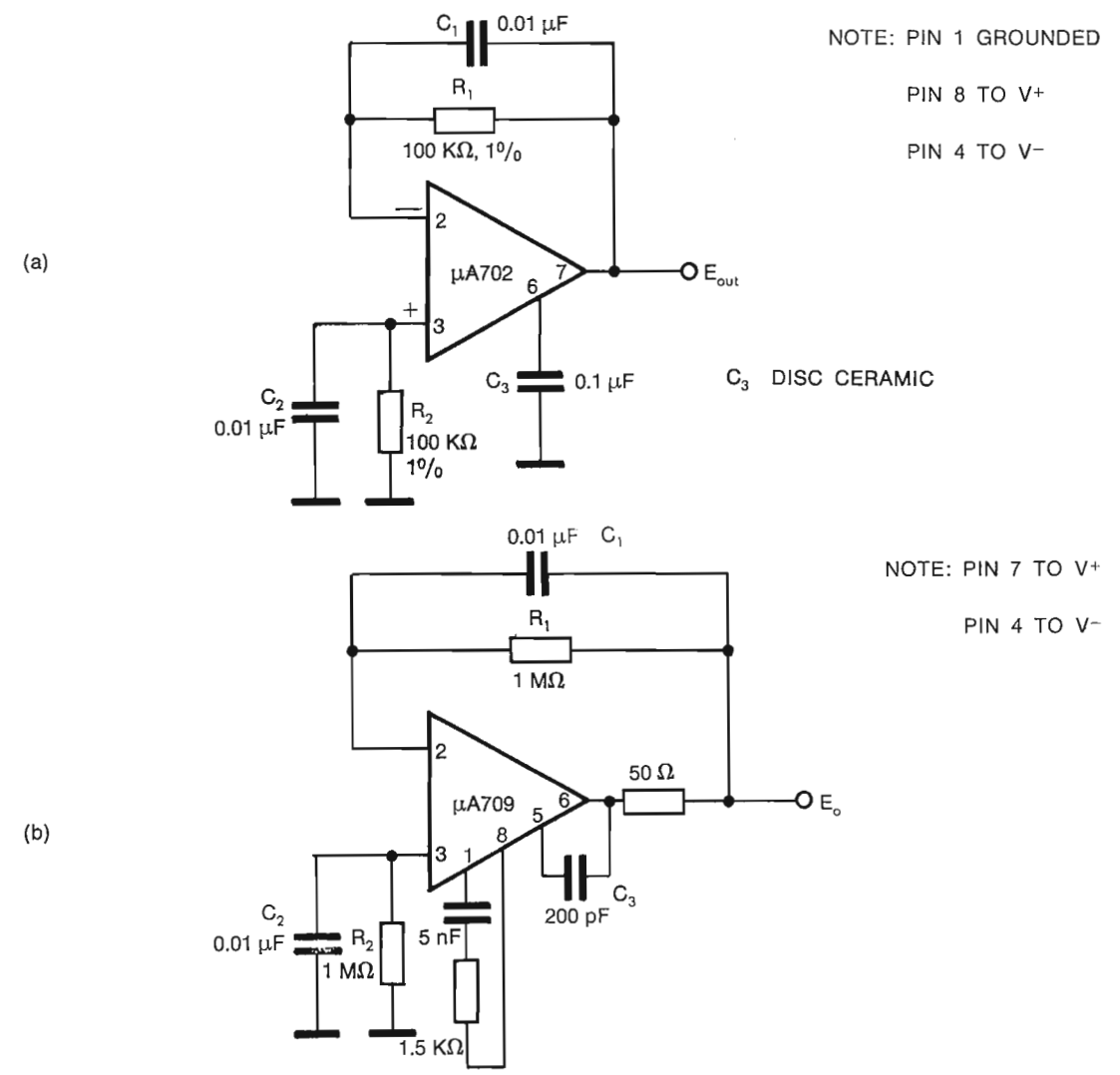


Fig. 4.5 - Circuit for Measuring Input Offset Current

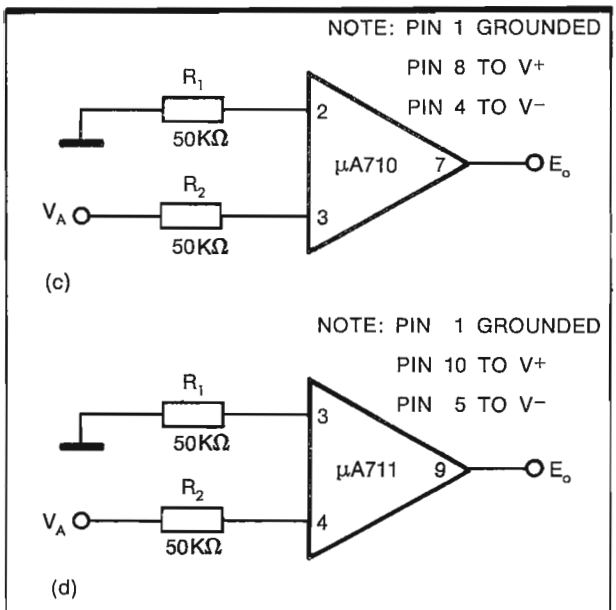


Fig. 4.5 - Circuit for Measuring Input Offset Current

4.2.5 Input Bias Current

Input bias current is defined as the average between the two currents flowing into the input terminals.

This value may be obtained using a D.C. current meter connected in series with one of the two paralleled resistors R_1 and R_2.

If R_1 and R_2 are equal and the internal resistance of the D.C. current meter is much lower than R_1 and R_2 the resistors divide the input current into two equal halves.

The meter indicated value is therefore the direct value of the bias current.

Bias current is defined for a certain value of supply voltage and at a fixed ambient temperature. The full scale of the D.C. current meter and the values of the resistors R_1 and R_2 depend on the particular integrated circuit as shown in Fig. 4.6 (a) (b) (c) (d).

Finally, for the dual differential comparator μA711 the test must be repeated for each side, with the other disabled, and with the strobe to ground.

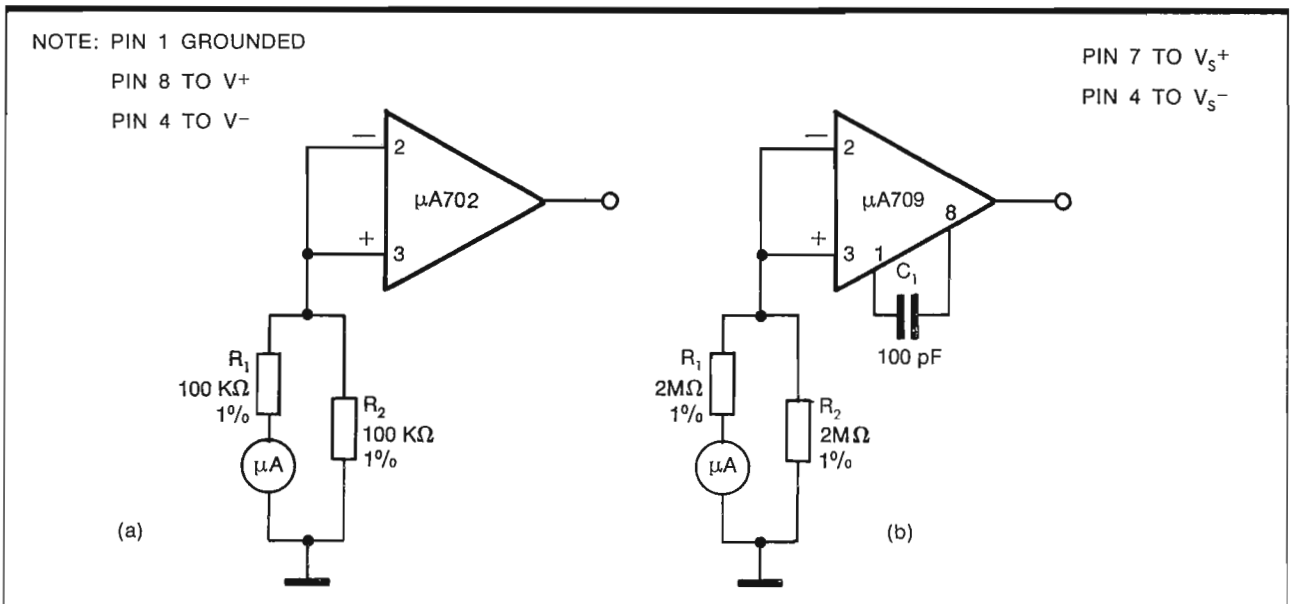


Fig. 4.6 - Circuit for Measuring Input Bias Current

4.2.6 Supply Voltage Rejection Ratio

Defined as the ratio of the change in input offset voltage to the change in supply voltage producing it.

The circuits of Fig. 4.4 may be used to measure this parameter.

The positive or negative supply, or both, are varied by a known amount ΔV_S (± 10% of nominal value would be reasonable).

The change in input offset voltage expressed in microvolts is read and the value of the Supply Voltage Rejection Ratio (SVRR) is calculated from the relationship

$$SVRR = \frac{\Delta V_{offset}(\mu V)}{\Delta V_S(V)}$$

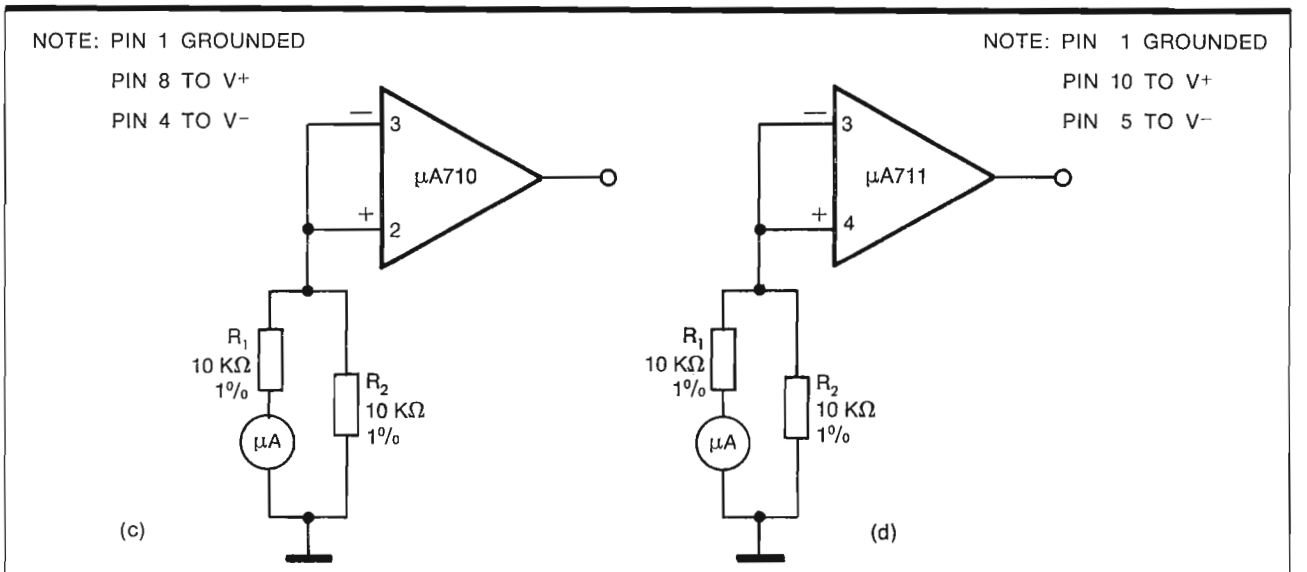


Fig. 4.6 - Circuit for Measuring Input Bias Current

5. FREQUENCY COMPENSATION

5.1 GENERAL

Frequency compensation is both desirable and necessary for many applications of integrated circuits which have been designed with high internal voltage gains. Apart from stability considerations, frequency compensation may be used to greatly reduce broad-band noise caused by the integrated circuit itself (see appropriate Section) or fed in at the input, if the bandwidth required by the amplifier is small compared with the maximum bandwidth obtainable.

Application of negative feedback to a high-gain amplifier gives a circuit with characteristics dependent almost entirely on the feedback elements. The improvement in gain stability, phase shift, input impedance, output impedance and linearity is proportional to the amount of feedback. Thus, amplification to any degree of accuracy is possible with sufficient feedback. Large amounts of feedback, however, require that close attention be given to the amplifier open-loop characteristics. Stable circuits must have well defined open-loop gain and phase responses to frequencies far above the band of interest; 60 dB of feedback over a 10 kHz bandwidth, for example, requires controlled open-loop characteristics to over 10 MHz.

The frequency compensation networks required to stabilise the feedback amplifier depend on, among other things, the open-loop gain, the frequency response characteristics and the impedance at the compensation terminals of the amplifier. Specification of limits for each individual factor which affects the design of the frequency compensation networks will give an unnecessarily restrictive result, since variations in these factors correlate to some degree in an integrated circuit. It is better to treat the amplifier as a whole by specifying complete networks which guarantee stability for the full distribution of units.

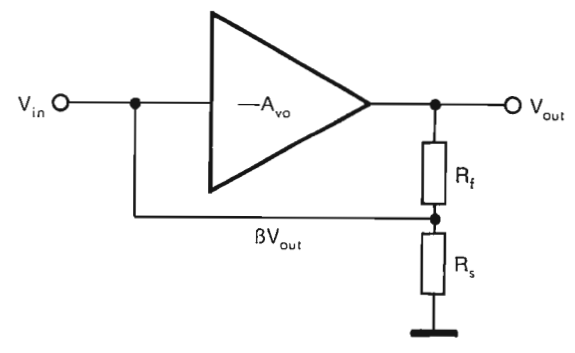


Fig. 5.1 - A Simple Feedback Amplifier

The closed-loop gain of the simple amplifier shown in Fig. 5.1 is given by:

$$A_v = -\frac{A_{vo}}{1 + \beta A_{vo}} \qquad \ldots\ldots\ldots\ldots(1)$$

Where A_v = Closed-loop voltage gain
A_{vo} = Open-loop voltage gain
β = Feedback factor

The quantity $(1 + \beta A_{vo})$ is the amount of feedback and is a direct measure of the improvement obtained in performance of the amplifier. This factor must be greater than zero for all frequencies if the circuit is to be stable. Hence the magnitude of loop gain, βA_{vo}, must be less than unity at the frequency where the loop phase-shift is 180°. For realβ, the maximum amount of feedback is limited to the ratio of the low-frequency value of A_{vo} and the value of A_{vo} ot the 180° phase-shift frequency.

5.2 μA702A OPERATIONAL AMPLIFIER

5.2.1 Lag Compensation

The open-loop gain and phase responses of a typical μA702A amplifier are shown in Fig. 5.2 including a straight line approximation to the actual curve. The gain rolls off at the 0.8 MHz first break frequency with a slope approaching 6 dB, per octave; a second break occurs at approximately 4 MHz, and a third break at 40 MHz. The 180° phase-shift frequency is about 14 MHz, so no more than 34 dB of feedback may be applied without oscillation.

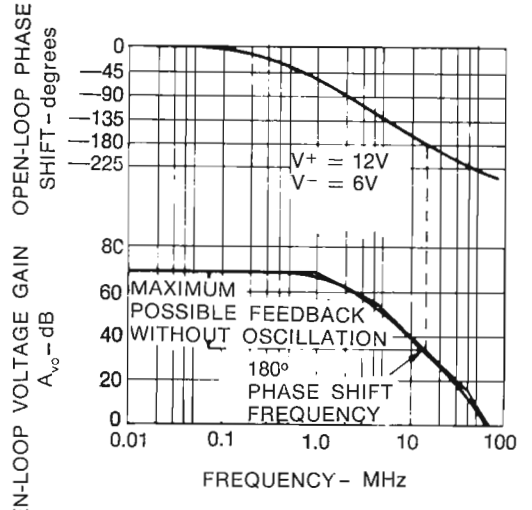


Fig. 5.2 - Typical Open-loop Gain and Phase Shift of the μA702A

It would not be practical to use this much feedback, however, since it is inevitable that the 180° phase-shift will be exceeded by minor deviations in the amplifier or external circuitry. Therefore, the limiting phase for maximum feedback should be chosen less than 180° by some definite margin to allow for variations in amplifier and circuit parameters.

Phase margins less than 90° will cause peaking in the closed-loop response at the frequency where the loop gain equals unity. This is because the magnitude of the denominator of Equation (1) becomes less than unity due to phase shift in βA_{vo}. The degree of peaking for various phase margins is shown in Fig. 5.3. A satisfactory circuit should have a minimum phase margin of 45° (less than 3 dB peaking). Thus only 20 dB of feedback can safely be applied to the basic amplifier.

Since the amplifier response is limited by internal capacitances, little can be done to increase the amount of feedback without purposely narrowing the open-loop bandwidth. The simplest way of designing a feedback amplifier which is stable with large amounts of feedback is to shunt some signal point in the circuit to ground with a single, relatively large, capacitor. If the roll-off due to this capacitor begins at a low enough frequency, the loop gain can be made less than unity before other circuit elements introduce additional phase shift. Since the maximum phase shift associated with a single RC network is 90°, the circuit cannot become unstable.

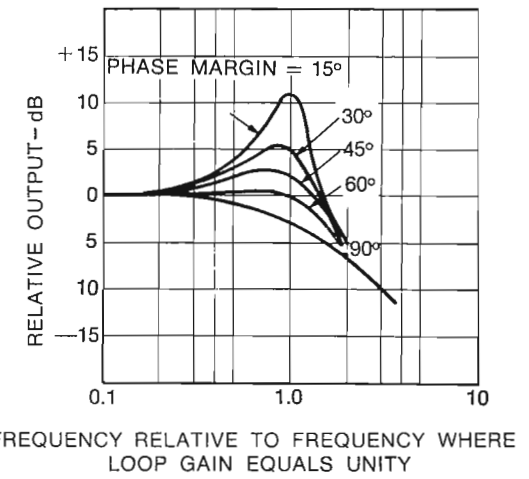


Fig. 5.3 - Peaking in Closed-loop Response for Various Phase Margins

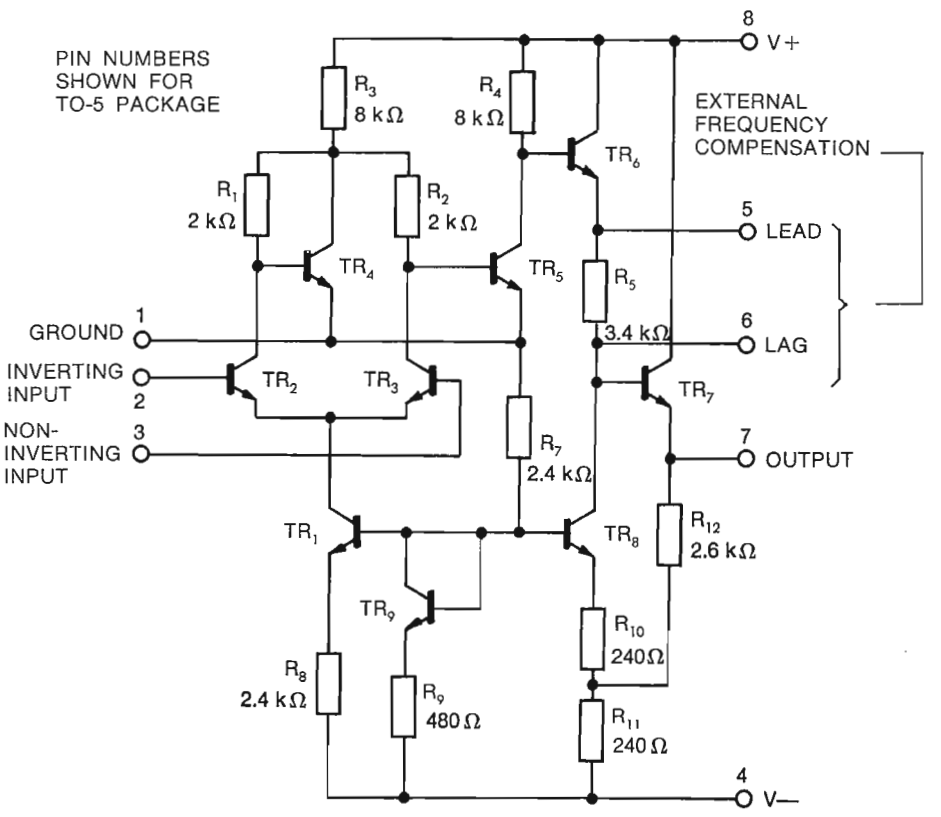


Fig. 5.4 - Circuit Diagram of the μA702A

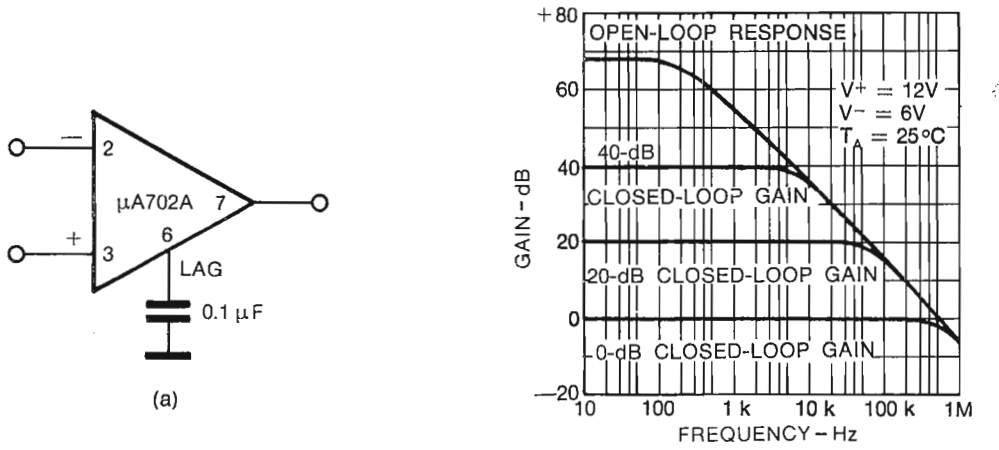


Fig. 5.5 - Frequency Response of the μA702A with Simple Lag Compensation

A point within the μA702A has been made available to facilitate this method of bandwidth narrowing. The circuit diagram of the amplifier is shown in Fig. 5.4; a capacitor connected from the lag compensation terminal to ground attenuates the high-frequency signals at the base of TR_7, giving the necessary roll-off in response. Fig. 5.5 shows the open-loop response of an amplifier using this frequency compensation and gives curves for various closed-loop gains.

Since the closed-loop circuit cannot supply more gain than is available from the amplifier itself, the closed-loop response intercepts and follows the open-loop gain curve at high frequencies, as shown in Fig. 5.5. Clearly, this circuit does not give maximum closed-loop bandwidth. It is ideal for D.C. applications, however, since frequencies above a few hundred cycles are ordinarily of little interest. The early roll-off in high-frequency gain not only reduces the broadband noise but makes the circuit less susceptible to instability caused by capacitive loading or stray capacitances in the feedback circuitry.

Maximum feedback over wide bandwidths can be obtained by using the natural roll-off of the amplifier to provide part of the compensation. This technique is illustrated by the circuit and loop gain response shown in Fig. 5.6. The series RC compensation network gives a roll-off in loop gain beginning at some lower frequency and breaking out at the natural roll-off frequency of the amplifier. The amplifier internal roll-off then provides the additional attenuation necessary to bring loop gain through unity with an adequate phase margin. This scheme gives the widest possible bandwidth for any value of closed-loop gain.

The values of the compensation components depend upon the loop gain, phase margin, and amplifier internal characteristics. The attenuation in loop gain from the compensation network is equal to the ratio of the internal resistance at the compensation terminal and the series compensation resistor; thus:

$$A_c = \frac{R_i}{R_1} \qquad \text{..... (2)}$$

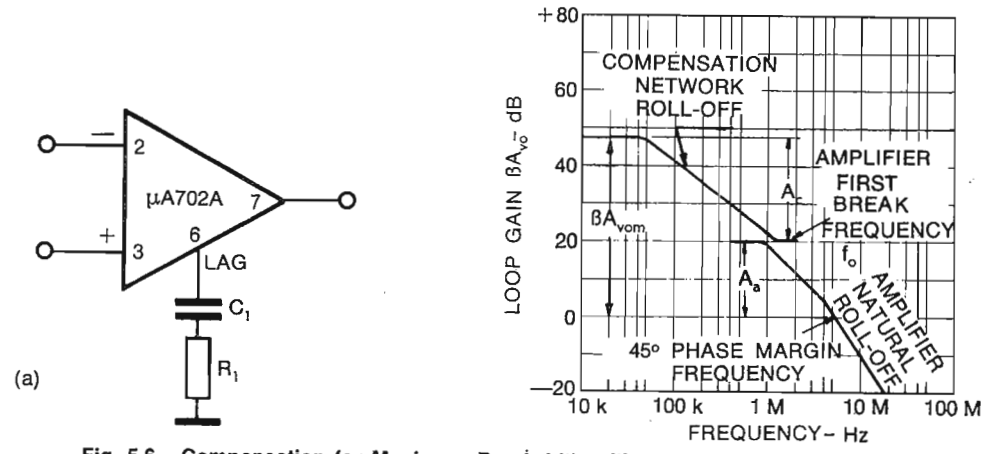


Fig. 5.6 - Compensation for Maximum Bandwidth with Lag Network

Where A_c = Attenuation in loop gain from compensation network
R_l = Amplifier internal resistance at the lag compensation terminal

The total attenuation from both compensation amplifier roll-offs must be equal to the low-frequency loop gain.

$$\beta A_{vom} = A_c A_a \qquad \text{..... (3)}$$

Where
A_a = Magnitude of low-frequency loop gain with some source resistance
A_{vom} = Attenuation in loop gain from the amplifier internal roll-off for a given phase margin

Therefore, the required value of compensation resistors is:

$$R_1 = R_i \frac{A_a}{\beta A_{vom}} \qquad \text{..... (4)}$$

The breakout frequency of the compensation network response should be made equal to the amplifier natural roll-off frequency for maximum feedback bandwidth, hence the value of the compensation capacitor is:

$$C_1 = \frac{1}{2\pi f_o R_1} \qquad \text{..... (5)}$$

Where f_o = First break frequency of the open-loop response.

A generalised feedback circuit for the amplifier is shown in Fig. 5.7

Single-ended signals may be applied to either input terminal if the resistor at the unused input is returned to ground. The total D.C. resistance to ground from each input should be equal for minimum D.C. offset at the output. The loop for the circuit of Fig. 5.7 is given by:

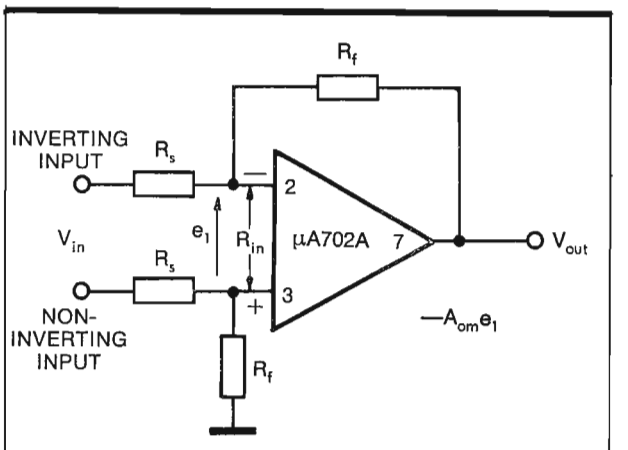


Fig. 5.7 - General Feedback Circuit

$$\beta A_{vom} = \left[\frac{1}{1 + \frac{R_f}{R_s}}\right]\left[\frac{A_{om}R_{in}}{R_{in} + 2\frac{R_f R_s}{(R_f + R_s)}}\right] \qquad \text{..... (6)}$$

Where A_{om} = Open-loop low-frequency gain measured with zero source resistances
R_{in} = Input resistance

This compensation will give stable closed-loop gain for the full production distribution of units.

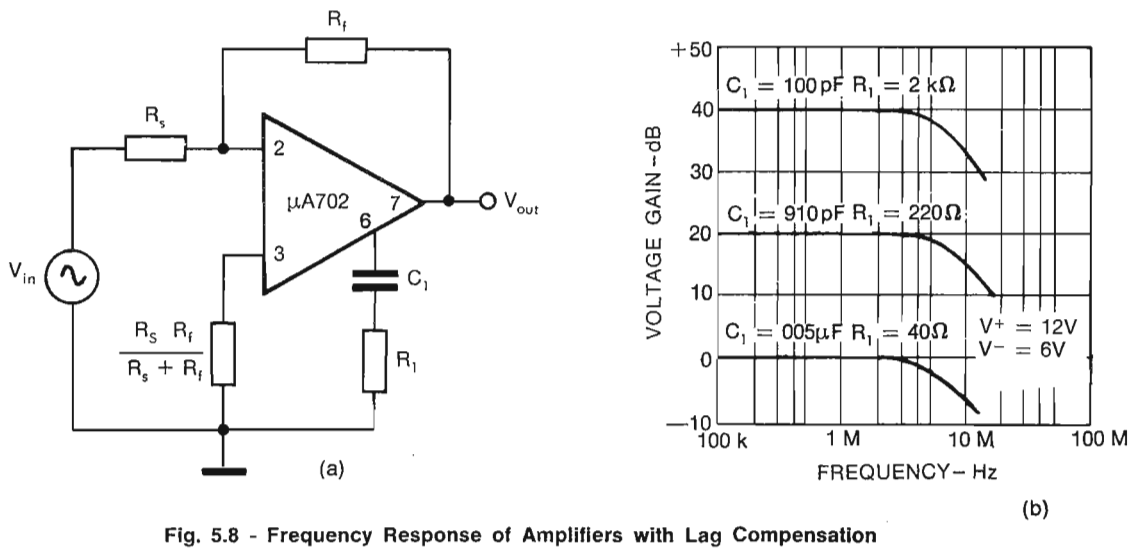


Fig. 5.8 - Frequency Response of Amplifiers with Lag Compensation

Examples of the closed-loop response obtained, using the recommended frequency compensation, are given in Fig. 5.8. The bandwidth can be expected to vary from 4 MHz to 10 MHz with less than 3 dB of peaking, depending upon the particular unit.

The source and feedback resistors should be kept as small as possible for maximum bandwidth. High resistances reduce the bandwidth because of finite amplifier input resistance and stray capacitance shunting the feedback resistor. If maximum bandwidth is not required, additional stability margin can be obtained by reducind R_1 and increasing C_1.

The frequency response of the μA702A is primarily a function of the collector-base capacitance of the integrated transistors, resistance values and the stage gains. Since these parameters are temperature sensitive, the bandwidth will change with temperature. Even though the absolute value of bandwidth varies, the ratio between the break frequencies does not change much. Thus, the circuit will be stable over wide temperature ranges. The change in closed-loop bandwidth with temperature is approximately —0.5% per degree centigrade for low-source resistances, as shown in Fig. 5.9. With high-source resistance, the bandwidth variation is offset by the change in loop-gain due to the temperature coefficient of the amplifier input resistance; hence, the relative change in closed-loop bandwidth is much less.

The effect of changes in the negative supply voltage on the bandwidth is shown in Fig. 5.10. If much variation in voltage is expected, the values of the compensation network components, as given in Equations (8) and (9) should be adjusted to give an adequate phase margin for the largest supply voltage anticipated. Dividing R_1 and multiplying C_1 by a factor of 1.5 to 2 will guarantee stability for voltages up to —9 V.

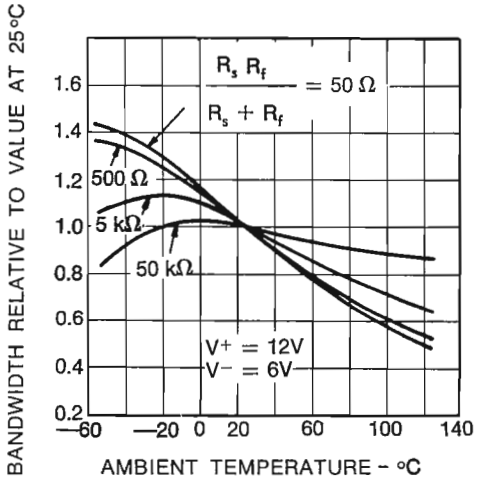


Fig. 5.9 - Effect to Temperature on Response of a Lag-Compensated Amplifier

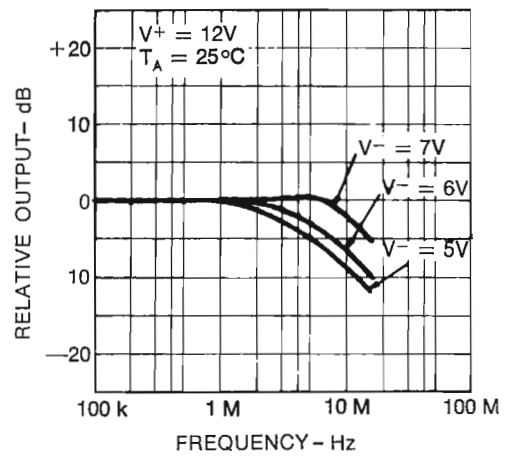


Fig. 5.10 - Effect of Negative Supply Voltage on Response of a Lag Compensated Amplifier

The bandwidth is not significantly affected by the positive supply voltage.

Excessive capacitive loading at the output of the feedback amplifier may cause peaking and possible instability. The capacitance breaking with the amplifier output resistance produces additional phase shift at the unity loop gain frequency, decreasing the phase margin. Since the compensation network is at the base of the output transistor, it reduces the high-frequency output impedance and makes the circuit less sensitive to capacitive loading. The effect of the load capacitance on the unity-gain amplifier is shown in Fig. 5.11. Selection of the compensation network values for stability with high capacitive loading may be done the same way as for supply voltage variations.

Equation (6) shows that the open-loop gain is decreased by circuit resistances which are larger than the amplifier input resistance. This affects the values of the compensation components if the widest possible bandwidth is desired. However, since R_{in} varies greatly with temperature, it is best to design the compensation network assuming that the loop gain is a maximum; this ensures stability for all conditions at the cost of some bandwidth with high circuit resistances. This is also important because high circuit resistances make stray capacitances more dominant. Therefore, using Equations (4) and (6), and assuming that

$$R_{in} \gg \frac{2R_sR_f}{R_s+R_f}$$

the expression for the compensation resistor becomes

$$R_1 = R_i \frac{A_o}{A_{om}} \left(1 + \frac{R_f}{R_s} \right) \qquad \ldots\ldots\ (7)$$

Since variations in the terms R_i, A_{om} and A_a are correlated to some degree, a compensation network design using individual limits for these parameters would be unnecessarily restrictive. It is better to specify the compensation taking the entire quantity

$$R_i \frac{A_a}{A_{om}}$$

as a single variable. Thus the distribution of this quantity, rather than the distribution of the separate terms, should be used in determining the values of the compensation components. Measurement of a large number of circuits gives the following design equations for the compensation network:

$$R_1 = 20 \left(1 + \frac{R_f}{R_s} \right) \Omega \qquad \ldots\ldots (8)$$

$$C_1 = \frac{0.01}{1 + \frac{R_f}{R_s}} \mu F \qquad \ldots\ldots\ldots (9)$$

5.2.2 Input Lag Compensation

A significant disadvantage of frequency compensating near the output of the amplifier is that the maximum high-frequency output voltage swing

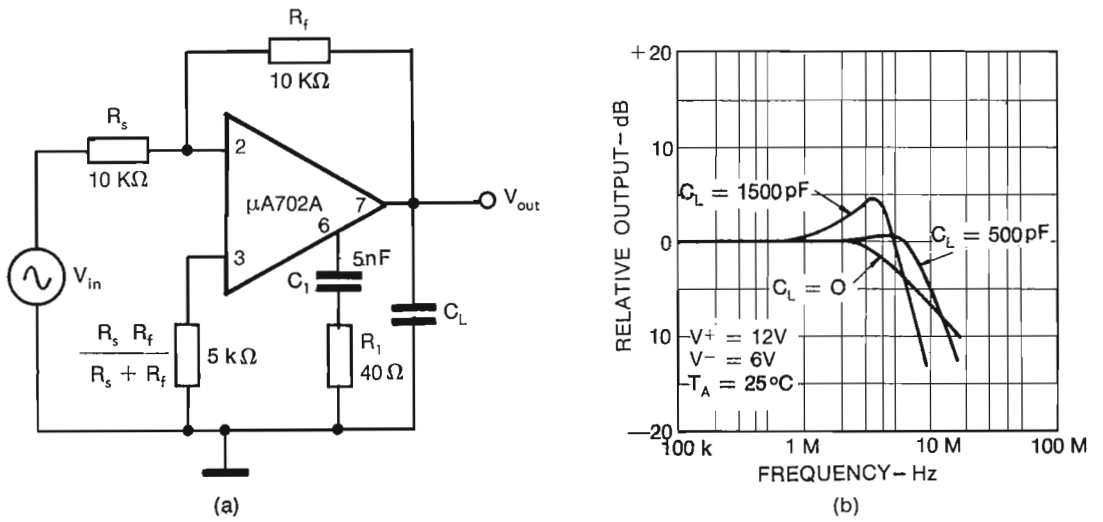


Fig. 5.11 - Effect of Load Capacitance on Response of a Unity- Gain Lag- Compensated Amplifier

is reduced by the compensation network Fig. 5.12. Since the compensation terminal is at a high-impedance, high-signal level point within the circuit, shunting the load impedance of TR_6 (Fig. 5.4) with the compensation network produces a proportional decrease in the peak undistorted voltage swing of this stage. Hence, full output swing can be obtained up to only the compensated open-loop bandwidth of the amplifier.

This limitation may overcome by placing the compensation network at a low level point in the system. Connection of the network across the input terminals, as in Fig. 5.13, permits the full output swing capability of the amplifier to be utilised. The attenuation in loop gain from the input compensation network is given by:

$$A_e = \left[\frac{\frac{2R_sR_f}{R_s+R_f}}{R_2} \right] \left[\frac{R_{in}}{R_{in} + 2\frac{R_sR_f}{R_s+R_f}} \right] \qquad \ldots\ldots (10)$$

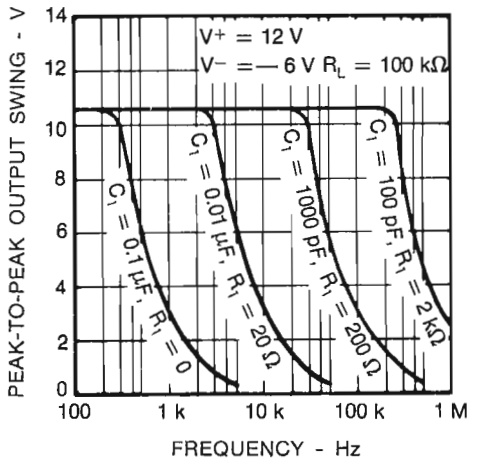


Fig. 5.12 - Output Voltage Swing as a Function of Frequency for Various Lag Compensation Networks

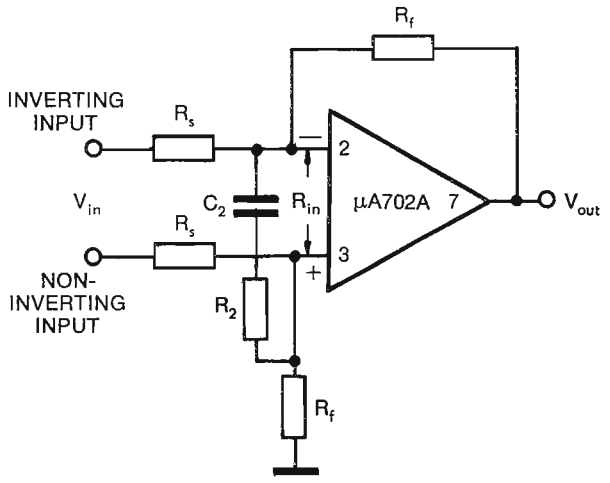


Fig. 5.13 - Amplifier with Lag Compensation at the Input

where $R_{in} \gg R_2 \ll 2\dfrac{R_sR_f}{R_s+R_f}$

From Equations (3), (5), (6) and (10), the compensation components are:

$$R_2 = 2R_f\frac{A_a}{A_{om}} \qquad \text{..... (11)}$$

$$C_2 = \frac{A_{om}}{4\pi f_o R_f A_a} \qquad \text{..... (12)}$$

These expressions show that the input compensation gives another advantage in addition to full output swing capability; the compensation is independent of the amplifier input resistance. This means that changes in input resistance will not affect the closed-loop bandwidth. Also, there will be less spread in bandwidth from unit to unit since the variations caused by R_i are eliminated.

The values for the compensation components are found in the same manner as for output lag compensation.

$$R_2 = 5\,R_f\Omega \qquad \text{..... (13)}$$

$$C_2 = \frac{0.04}{R_f}\ \mu F \qquad \text{..... (14)}$$

where R_f is in kilohms

5.2.3 Lead Compensation

Only lag compensation methods have been discussed so far. The μA702A, however, has an additional compensation point which can be used to put some leading phase shift into the open-loop

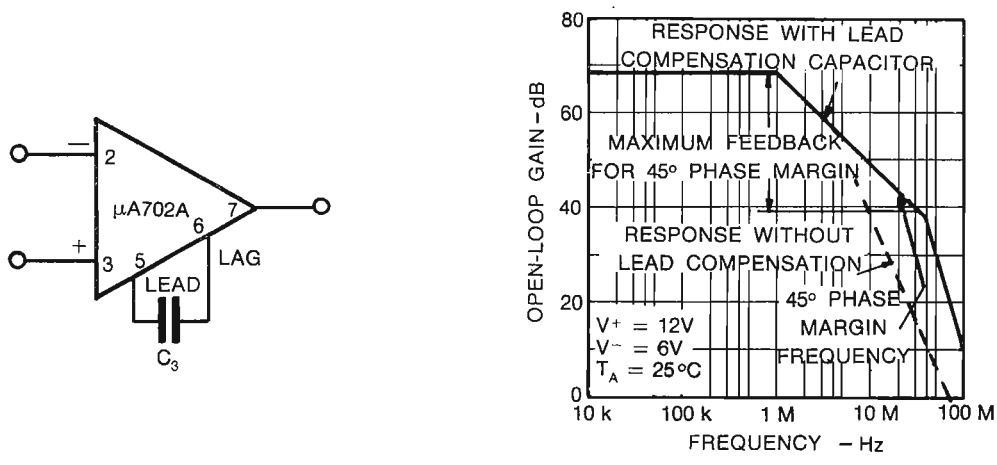


Fig. 5.14 - One-loop Frequency Response of μA702A with Lead Compensation

response and thus increase the useful bandwidth by about 2 octaves. Connecting a small capacitor across the lead-lag frequency compensation terminals (see Fig. 5.4), effectively moves the second break point in the open-loop frequency response to a much higher frequency. This gives a frequency response shown in Fig. 5.14, about 30 dB of feedback may be used for a 45° minimum phase margin. Thus 10 dB more feedback can be obtained than for lag compensation only, and the bandwidth is about four times as large.

The optimum value for the lead compensation capacitor is about 50 pF to 100 pF.

Closed-loop gains less than 40 dB require additional lag compensation. This is best placed at the input, both to reduce the effective input impedance and to maintain a large high-frequency output swing capability. The design equations for the lag compensation components are:

$$R_2 = 20R_f\Omega \qquad \text{..... (15)}$$

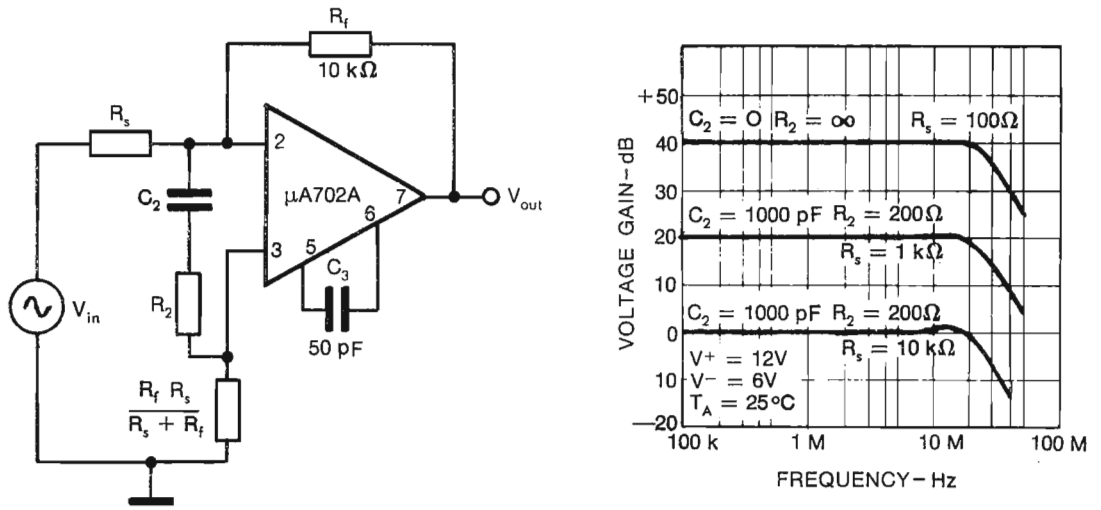


Fig. 5.15 - Frequency Response of Lead Compensated Amplifier

$$C_2 = \frac{0.01}{R_f}\ \mu F \qquad \text{..... (16)}$$

where R_f is in kilohms.

Examples of the closed-loop responses obtained, using both lead and lag compensation are shown in Fig. 5.15. The bandwidth will vary from 12 MHz to 40 MHz depending upon the open-loop gain and bandwidth of the particular unit.

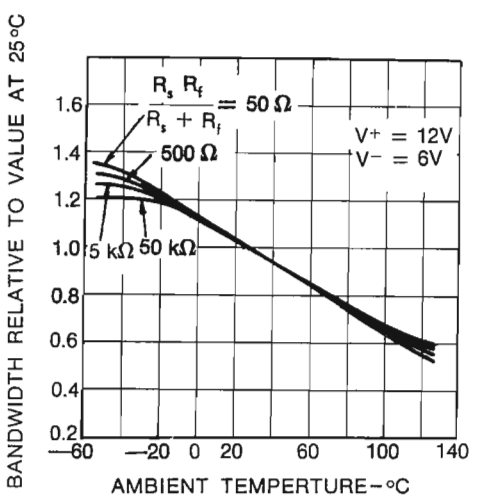


Fig. 5.16 - Effect of Temperature on Response of a Lead-Compensated Amplifier

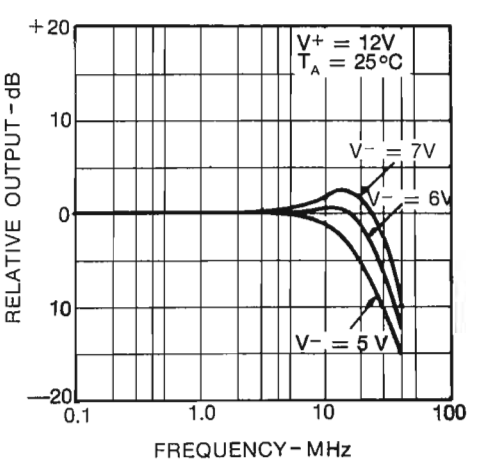


Fig. 5.17 - Effect of Negative Supply Voltage on Response of a Lead - Compensated Amplifier

With the large bandwidths possible using this compensation, it is extremely important to keep the impedance levels low to avoid undesirable effects due to stray capacitance. Only 0.5 pF across a 30 kΩ feedback resistor, for example, will reduce the bandwidth to 10 MHz.

The relative change of bandwidth with temperature is shown in Fig. 5.16. The independance of bandwidth from source and input resistances is evident. The effect of negative supply voltage, Fig. 5.17, is about the same as for output lag compensation.

The circuit is considerably more sensitive to capacitive loading, however, since the bandwith is so much larger. The peaking due to load capacitance, see Fig. 5.18, may be reduced by shunting the feedback resistor with a very small capacitor or by increasing the lead capacitor to about 500 pF. This is effective if the load capacitor isn't too large and is relatively constant. For load capacitances greater than about 100 pF, it is best to increase the phase margin by dividing R_2 and multiplying C_2 by a factor of 2 or more.

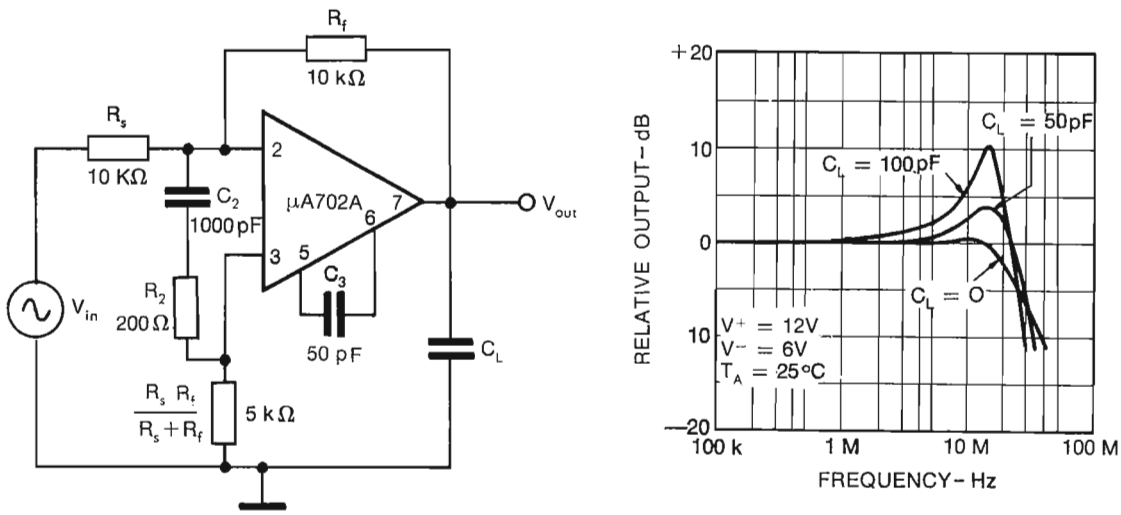


Fig. 5.18 - Effect of Load Capacitance on Response of a Unity-Gain Lead-Compensated Amplifier

5.2.4 Other Circuits

The design equations derived for the frequency compensation networks are sufficiently conservative to guarantee stability for the full production distribution of μA702As. For certain specific applications or for a few selected units, it may be advantageus to experimentally determine the optimum compensation for maximum bandwidth. The proper procedure is to measure the loop gain response with the circuit of Fig. 5.19, adjusting the compensation for the desired phase margin at the unity loop gain point.

Thus maximum bandwidth can be obtained for given conditions of supply voltages, temperature, loading, and other circuit variables.

The compensation components for operation at +6 V and —3 V supplies are readly colculated for the + 12 V and — 6 V values. The open-loop frequency response and internal impedances are fairly constant with alteration of supply voltages; the only important change is that the open-loop voltage gain is about 10 dB less. Hence, the proper values for the lag networks may be found by multiplying R and dividing C by a factor of 3. The 50 pF lead compensation capacitor remains the same. Following this procedure gives essentially the same bandwidths and stability margin as for high-voltage supplies.

The output should be monitored with a high-gain, wide-band oscilloscope to make sure that the circuit is not oscillating before proceeding with the measurements.

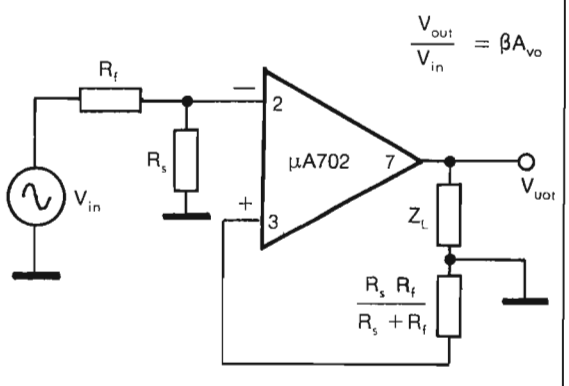


Fig. 5.19 - Circuit for Measuring Loop-Gain

5.2.5 « Slewing » Rate versus Noise Considerations

It has been shown in the previous paragraphs that the μA702A may be frequency compensated by having an RC network placed between the lag terminal and ground or across the input terminals (between pins 2 and 3). The choice of either of these solutions with the appropriate values for the network enables the same bandwidth for the amplifier to be obtained. However, the resulting characteristics of the amplifier, with regard to noise and rate of output voltage swing (slewing rate) are very different.

The frequency response characteristics of an amplifier having a large output signal swing can be described as the « slewing rate » (V/μsec.) or the response for full output swing. The « slewing rate » is defined as the maximum gradient for the rate of change of output voltage. With knowledge of the response at full output, a maximum frequency may be specified for which it is possible to have an undistorted sinusoidal output voltage equal in amplitude to that at low frequency. Obviously these two parameters are correlated.

The largest value of slewing rate is obtained with compensation at the input, the smallest value with compensation at the output, while with a combined form of compensation it is possible to cover the intermediate values.

In order to investigate the effects on « slewing rate » according to the position of the compensation, suppose that a square wave is injected into the input of an amplifier compensated at the output, with sufficiently small amplitude to maintain the amplifier working in a linear region. Under these conditions, due to the effect of negative feedback, the output rise-times are determined by the shape of the closed-loop passband.

If the amplitude of the waveform, at the input, is increased beyound the value for which the output of the amplifier is linear, the effect of the feedback resistor becomes almost negligible; the thing which determines the rise-time, for positive-going signals, is the time constant R_iC_1 (i.e. the open-loop passband of the compensated amplifier), and for negative-going it is the maximum current which is able to be absorbed by the transistor TR_8. (See Fig. 5.4 and 5.20 (a) in which C_1 is the compensating capacitor).

It can be seen that transposing the compensation from the output to the input improves the « slewing rate » since the amplitude of the signal is progressively reduced, whilst the compensation RC time-constant value remains fixed.

Considering the case of the μA702A with compensation directly across the input terminals, the rise-time for an output square wave of small amplitude is determined by the closed-loop frequency response whilst for large signals it is limited only by the open-loop frequency response of the uncompensated amplifier.

Where a combined compensation is used (Fig. 5.20 (b) and (c)), it is the capacitor C_1 at the output which determines the characteristics of the « slewing rate » (slower than with compensation only at the input). Nevertheless, since C_1 is smaller in value than C_1 in Fig. 5.20 (a), a better response is obtained than in the case of only the single compensation network at the output.

The noise characteristics are also dependent on the position of the compensation networks. The best characteristics are obtained with compensation at the output, in which case, the noise and signal are attenuated to the same extent.

Compensation at the input, on the other hand, appreciably worsens the signal-to-noise ratio, since the RC compensation network acts only on the signal, whilst not attenuating the noise introduced within the various stages of the amplifier. Hence, in this case, a combined form of compensation gives an intermediate characteristic between those of the two previous cases.

It may be seen that the use of lead compensation alone (i.e. placing a capacitor of 50 pF to 100 pF between pins 5 and 6 — see Section 5.2.3) does not sensibly alter the characteristics from that of an open-loop amplifier.

In Fig. 5.20 (a), (b), (c) and (d) are shown the circuits for inverting amplifiers with closed-loop gains of ten and with a passband of approx. 5 MHz.

They differ only in the type of compensation. The formulae for the component values are shown beside each figure and are calculated taking into account parameter tolerance in the μA702A as described in Sections 5.2.1 and 5.2.2.

In the case of the combined frequency compensation as shown in Fig. 5.20 (b) and (c) the formulae are derived as follows.

The first time-constant (break-point frequency f_1 of the compensated response curve) is determined by the capacitance C'_2 thus:

C'_2 equals C_2

The resistor R'_2, used in conjuction with capacitor C'_2, gives the choice of introducing a « zero » at a frequency between f_1 and f_o (where f_o is the first break-point frequency of the open-loop response).

Putting $f_2 = \dfrac{f_o}{K}$ the resistance R'_2 is given by:

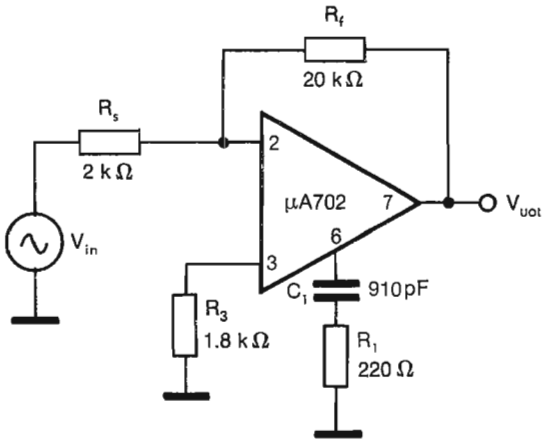
$R'_2 = KR_2$

where the limits for variation of the constant K are defined by the relationship:

$f_1 < f_2 < f_o$

Thus giving:

$$f_1 = \frac{1}{4\pi \dfrac{R_sR_f}{R_s+R_f} \cdot C_2} = \frac{f_o}{\dfrac{R_s}{R_s+R_f} \cdot \dfrac{A_{om}}{A_o}} = \frac{f_o}{\dfrac{R_s}{R_s+R_f} \cdot 200}$$

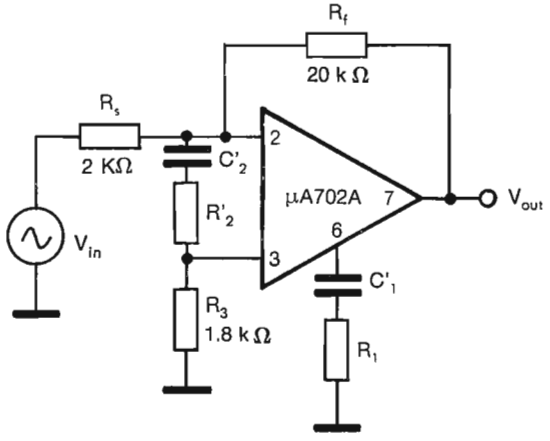


$$R_3 = R_s \| R_f$$

$$R_1 = 20 \left(1 + \frac{R_f}{R_s} \right) = 220\,\Omega$$

$$C_1 = \frac{0.01}{1 + \frac{R_f}{R_s}}\ \mu F = 910\ pF$$

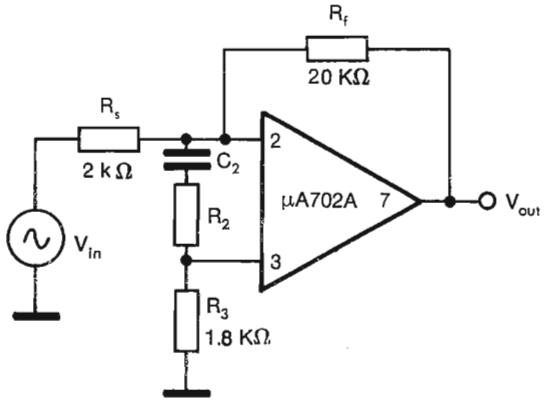
(a) Output Lag Compensation



$R_3 = R_s \| R_f$

For K > 1	b K = 10	c K = 5
$C'_2 = C_2 =$	2000 pF	2000 pF
$R'_2 = KR_2 =$	1000 Ω	500 Ω
$C'_1 = 50\ pF \cdot K =$	500 pF	250 pF
$R'_1 = \frac{4000\,\Omega}{K} =$	400 Ω	800 Ω

(b) and (c) Input and Output Compensation



$$R_3 = R_s \| R_f$$

$$R_2 = 5\,R_f = 100\,\Omega$$

$$C_2 = \frac{0.04}{R_f}\ \mu F = 2000\ pF$$

(R_f in Kilohms)

(d) Input Lag Compensation

Fig. 5.20 - Frequency Compensation Networks for a x10 Amplifier

From these equations the limits of K may be re-written as:

$$200 \frac{R_s}{R_s + R_f} > K > 1$$

The capacitor C'_1 gives the choice of introducing, in conjuction with resistor R_1, a « pole » at the frequency $\frac{f_o}{K}$ from which

$$C'_1 = \frac{1}{2\pi f_o / K R_i} = 50 \text{ KpF}$$

The resistor R'_1, together with capacitor C'_1, must introduce a « zero » corresponding to the appropriate break-point frequency (f_o) of the amplifier. Thus:

$$R'_1 = \frac{1}{2\pi f_o C'_1} = \frac{1}{2\pi f_o \cdot \frac{1}{2\pi f_o / K R_i}} = \frac{R_i}{K} = \frac{4000}{K} \Omega$$

As in the previous cases examined, if a larger stability margin is required it is sufficient to increase the capacitor value and reduce the resistance by the same factor.

THE EXPERIMENTAL RESULTS

Table 1 shows the measured noise characteristics and « slewing rate » for the amplifiers of Fig. 5.20. These give excellent experimental confirmation of the considerations discussed in the previous paragraphs.

It can be seen how the noise is increased by a factor of 10 by transposing the compensation from the output to the input, whilst the large signal output voltage increases to coincide with that of the open-loop amplifier. In addition, it can be seen how combined compensation gives a reasonable compromise between various requirements.

Finally, it must be realised, that the change in characteristics between case (a) and case (d), very noticeable where the gain is 10, is progressively reduced with increase in closed-loop gain and shows a maximum difference for an amplifier approaching unity gain.

Thus, it is the compensation capacitor which, for the most part, is responsible for the noise and « slewing rate » characteristics becoming increasingly so with reduction of closed-loop gain.

Type	Noise referred to the Input (measured over an effective bandwidth of 1.57 MHz) µV eff	Response at full Output Voltage Swing (±5 V) KHz	Slewing Rate V/µsec.
a	14.8	10	0.35
b (K=10)	32	20	0.7
c (K=5)	53	40	1.5
d	170	800	30

Table 1 - Dependance of Amplifier Characteristics on Position of Frequency Compensation

5.2.6 Special Precautions

Most problems encountered in the use of the µA702A are caused by poor circuit layout and inadequate power-supply bypassing. It should be kept in mind that the amplifier is potentially unstable to almost 100 MHz since it has greater than unity gain below this frequency. Therefore, care should be taken in connecting the amplifier to external equipment to make sure that prasitic oscillations do not occur. This applies to D.C. circuits as well as to 30 MHz. amplifiers.

Of particular importance is power-supply bypassing, as is the case with any high-gain feedback amplifier. Positive feedback through excessive impedance in the power supplies may cause very high frequency internal oscillations in the amplifier. This type of oscillation generally makes itself known by unreasonable D.C. performance of the amplifier, i.e., the output now may be extremely sensitive to power supply voltage changes, common-mode inputs or signal polarity. Bypassing the power supplies immediatly adjacent to the amplifier lead-out wires with 0.01 µF to 0.1 µF low-inductance capacitors should eliminate this form of possible instability.

If the circuit layout is not neat, stray capacitance from the output to the inputs may cause excessive peaking in the response or actual oscillations. Even with a neat layout, the unavoidable stray capacitance may cause problems if the source resistances are high. This may be cured by using an inverting amplifier configuration and bypassing the non-inverting input to ground with 50 pF to 100 pF. This remedy cannot be used if the compensation network is at the input, however, but in this case the network reduces the effective input impedance so that stray capacitance is less critical.

Some difficulty may be experienced when thermal tests are performed on the amplifier. The capacitive coupling between the long leads from the thermal test jig to the external circuit components can make the amplifier hard to stabilize. Under these circumstances it is mandatory to keep the leads as short as possible, with connections to the external circuitry made immediately outside the temperature chamber.

The frequency compensation network should be very conservative, and may be mounted directly on the amplifier socket together with the power-supply bypass capacitors.

5.3 μA709 OPERATIONAL AMPLIFIER

5.3.1 Lag Compensation

Practically all operational amplifiers require a frequency response compensation.

Two compensating points are provided in the μA709 element because of its high voltage gain; in fact it is normally difficult to obtain more than 60 dB attenuation with only one RC network.

The compensating points chosen feature a high internal resistance so that the amplifier can be compensated with small external capacitors.

The μA709 device cannot be used in open-loop configuration without any compensating network, because oscillations occur.

To avoid this drawback two capacitors are required: one $C_1 = 10$ pF between pins 1 and 8 and the other $C_2 = 3$ pF between pins 5 and 6 (Fig. 2.32 Section 2.5.3).

This is due to an internal feedback network (comprising R_7 and R_{15}) and to the difficulty of avoiding parasitic oscillations in amplifiers with a high gain at high frequencies.

The frequency compensation is obtained by an RC network connected between pins 1 and 8 and a capacitor C_2 between pins 5 and 6 (Fig. 5.21).

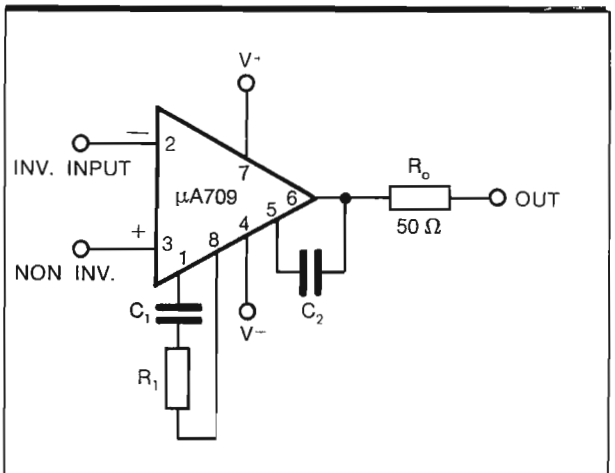


Fig. 5.21 - Frequency Compensation Circuit

Capacitor C_1 introduces a pole in the open-loop network at a frequency given by:

$$f_1 = \frac{1}{2\pi C_1 A_2 R_{i1}} \qquad \text{..... (1)}$$

where:

R_{i1} is the resistance between pin 1 and ground.

A_2 is the μA709 second stage voltage gain (TR_4, TR_6).

Resistor R_1 in series with capacitor C_1 introduces a zero at a frequency:

$$f_2 = \frac{1}{2\pi C_1 R_1} \qquad \text{..... (2)}$$

limiting the high-frequency attenuation introduced by the R_1 C_1 network at a value defined by:

$$A_C = \frac{R_{i1} A_2}{R_1} \qquad \text{..... (3)}$$

The amount of such an attenuation is kept constant in different cases.

Finally, capacitor C_2 is chosen in order to introduce a pole at frequency f_2 such as to eliminate the effect of the zero introduced by resistor R_1 and to allow an open-loop response with an unity slope (20 dB/dec).

Hence:

$$C_2 = \frac{1}{2\pi f_2 R_{i5} A_4} \qquad \text{..... (4)}$$

where:

R_{i5} is the resistance between pin 5 to ground.

A_4 is is the last-stage-but-one (TR_{12}) voltage gain.

The total attenuation introduced by the compensation networks has to be equal to the loop-gain, hence

$$\beta A_{vom} = A_c A_a \frac{f_a}{f_1} \qquad \text{..... (5)}$$

where:

A_{vom} is the voltage gain with the source resistance R_S;

A_a is the attenuation due to the output compensating network;

f_a is the frequency which makes the loop-gain equal to 1.

At frequency f_a the amplifier has to show a phase margin enough to avoid oscillations or overshoots in the step response.

Solving the previous equations with respect to R_1, S_1 and C_2 we obtain:

$$C_1 = \frac{5 \cdot 10^{-8}}{1 + \frac{R_f}{R_s}} \mu F \qquad \text{..... (6)}$$

$$C_2 = \frac{2 \cdot 10^{-4}}{1 + \frac{R_f}{R_s}} \mu F \qquad \text{..... (7)}$$

$R_1 = 1.5\ k\Omega$

The amount of the attenuation A_c, which is constant for the different conditions, and hence the value of R_1, has been chosen in order that the frequency compensation does not appreciably affect the amplifier noise performance, and that capacitors C_1 and C_2 have roughly the same effect on the slewing rate.

Fig. 5.22 shows the small-signal open-loop gain for different values of the compensating network

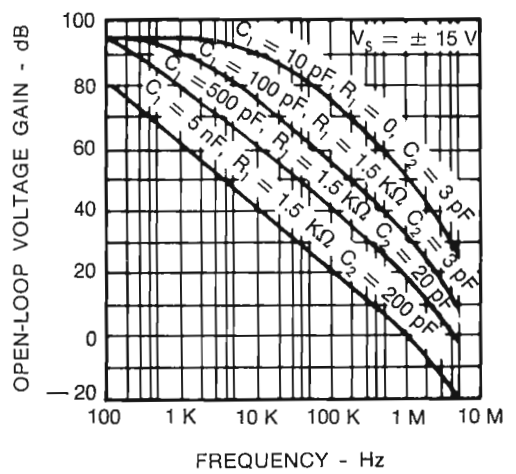


Fig. 5.22 - Open-Loop Frequency Response for Various Values of Compensation

It should be noted, that in presence of very small capacitive loads (50 pF - 100 pF) oscillations at very high frequency (10 - 15 MHz) often occur.

Such oscillations generally happen only when the NPN transistor TR_{14} is conducting.

These oscillations are due to the internal feedback provided by resistors R_7 and R_{15} and can be eliminated by connecting a 50 Ω resistor in series with the μA709 output: this sufficiently insulates such an amplifier from capacitive loads.

This resistor does not appreciably affect the integrated amplifier performance and introduces only a slight increase in output impedance (from 150 Ω to 200 Ω).

The frequency compensation described, is suitable in many respects: (small capacitance, values, independence from external resistance values, negligible influence in noise performance) but has the drawback of reducing the maximum output swing at high frequency.

Fig. 5.23 shows the maximum peak-to-peak voltage as a function of the frequency which can be obtained at the output for different values of compensation networks.

The slewing rate is about 0.3 V/μsec. for a 20 dB/decade slope, over the unity gain point.

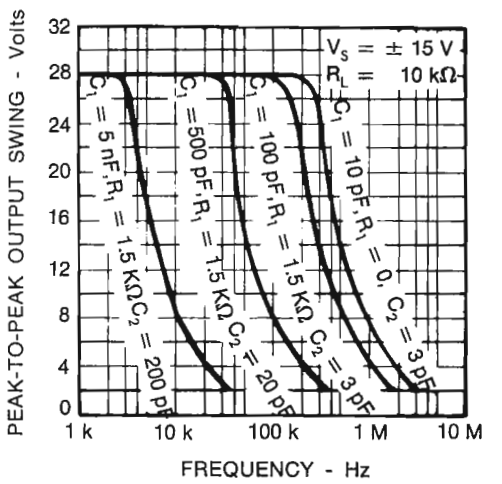


Fig. 5.23 - Output Voltage Swing as a Function of Frequency for Various Compensation Networks

5.3.2 Input Lag Compensation

In many applications, however, the reduction in output swing at high frequencies, due to the compensation already described, is unacceptable.

This limitation can be overcome using a compensation network, connected to the input pins, in addition to the ones connected between pins 1 and 8, 5 and 6, designed for the minimum values:

$C_1 = 10$ pF $\qquad R_1 = 0 \qquad C_2 = 3$ pF

The attenuation in the loop-gain introduced by the compensation network connected to the input pins, and comprising capacitor C_3 in series with the resistor R_3, is as follows:

$$A_c \cong \frac{2 R_s R_f}{(R_s + R_f) R_3} \qquad \text{..... (8)}$$

Hence from equations 5 and 8 we obtain:

$$R_3 = 2 \frac{A_a}{A_o} R_f = 20 R_f (\Omega) \qquad \ldots\ldots\ (9)$$

$$C_3 = \frac{A_o}{4 f_a R_f} = \frac{9}{R_f} (\mu F) \qquad \ldots\ldots\ldots\ (10)$$

where R_f is expressed in kilohms.

5.3.3 Intermediate Frequency Compensation

The input compensation, even though it improves the intrinsic slewing rate characteristic of the device, causes a worsening of the amplifier noise performance; which is considerable when the closed-loop gain approaches unity.

This is the reason why, in many cases, the use of compensation, which is a compromise between noise and slewing rate performance, is preferred.

A simple way to design the new networks is to choose C_1 and C_2 to obtain the required slewing rate: the necessary attenuation and stability with frequency being obtained by use of the network connected to the input.

Equation (8) gives the design criteria for the value of R_3 while the value of C_3 can be obtained from (10).

The amount of attenuation introduced by the RC network connected to the input indicates how the noise performance deteriorates.

Table 2 shows the experimental results of the unity-gain inverter amplifier shown in Fig. 5.24, for all the aforementioned configurations.

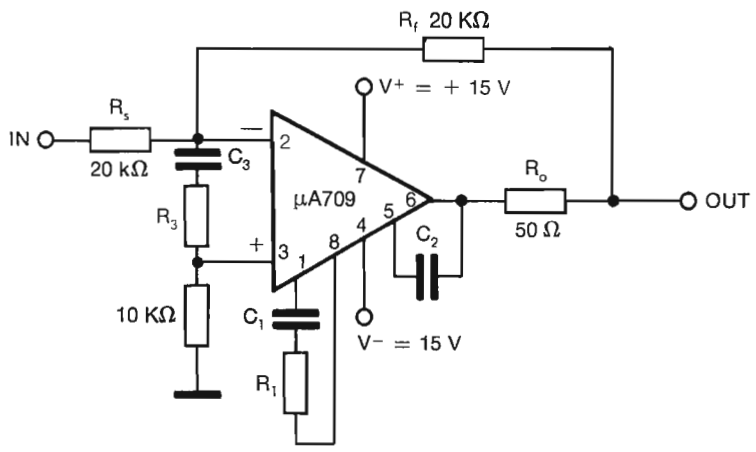


Fig. 5.24 - Unity Gain Inverting Amplifier

Kind of compensation	LAG COMPENSATION	INPUT LAG COMPENSATION	INTERMEDIATE FREQUENCY UNIT COMPENSATION	
	$R_1 = 1.5\ k\Omega$ $C_1 = 5000\ pF$ $C_2 = 200\ pF$	$R_3 = 39\ \Omega$ $C_3 = 0.47\ \mu F$ $C_1 = 10\ pF$ $C_2 = 3\ pF$ $R_1 = 0$	$C_3 = 0.47\ \mu F$ $R_3 = 1\ k\Omega$ $C_1 = 250\ pF$ $R_1 = 1.5\ k\Omega$ $C_2 = 10\ pF$	
Bandwidth (— 3 dB)	500	500	500	KHz
Full power response	4.5	300	80	KHz
Slewing Rate	0.3	22	6	V/μsec.
Noise Voltage	0.03	20	1.3	mVp-p.

Table 2

5.3.4 Frequency Response with a Slope Higher than 20 dB/dec.

In the preceding paragraphs, amplifiers having a unity slope (20 dB/dec.) frequency response have been considered, because the ones with a greater slope are, at first sight, more difficult to stabilize even if they offer some advantages with respect to conventional amplifiers.

The stabilization difficulties can be easily overcome with amplifiers having a frequency response slope of 40 dB/dec. for high gain values (≥40 dB), and a slope of 20 dB/dec. near the unity gain.

Fig. 5.25 shows the frequency response in both cases for the μA709 device, and the component values of the compensation networks.

It is evident that the amplifier with a slope greater than 20 dB/dec. has a higher open-loop gain at low frequencies.

Consequently in this region the amount of negative feedback is greater and hence it is possible to have higher closed loop-gain stability, lower distortion and a smaller output impedance.

The compensation capacitors are smaller, and this means shorter recovery times and reduced overall dimensions, therefore these amplifiers can exhibit higher slewing rates and better noise performance.

There are no problems concerning stability with frequency when the closed-loop gain is approximately unity, but there are overshoots in presence of step functions, and oscillations with higher gains.

These oscillations can, however, be eliminated by a small capacitor C_7 connected in parallel with the feedback resistor.

5.3.5 Other Circuits

The design criteria for the compensation network described in the preceding paragraphs ensure the maintenance of stability allowing for the 'spread' of parameters during manufacture of the semiconductors.

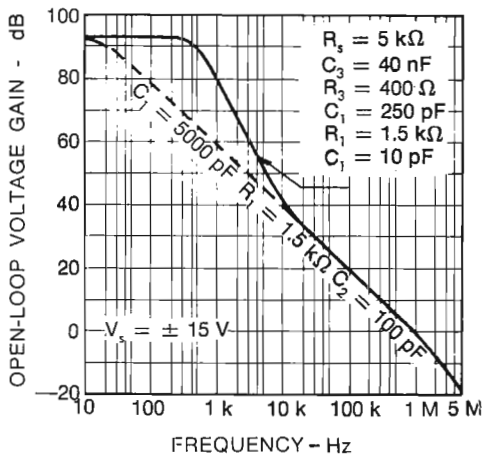
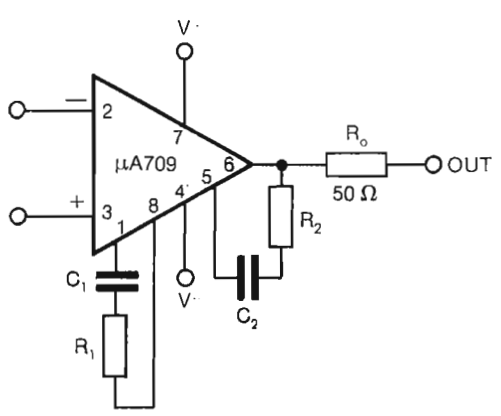


Fig. 5.25 - Comparison of 40 dB/dec and 20 dB/dec Open Loop Response of μA709

In some cases it might be convenient to use systems whose performance is not so exacting in order to achieve a larger bandwidth.

This is obtained, for instance, using the compensation shown in Fig. 5.26 (a) which differs from the one described in Section 5.3.1 because a resistor R_2 has been connected in series with the capacitor C_2 in order to compensate for the second pole which appears in the open-loop frequency response of Fig. 5.22.

Fig. 5.26 (b) shows the open-loop frequency response with such a compensation; it is evident that the improvement in both bandwidth and slewing rate characteristics by almost a factor of 5, in conjuction with a higher capacitive-load-sensitivity, is obtained.



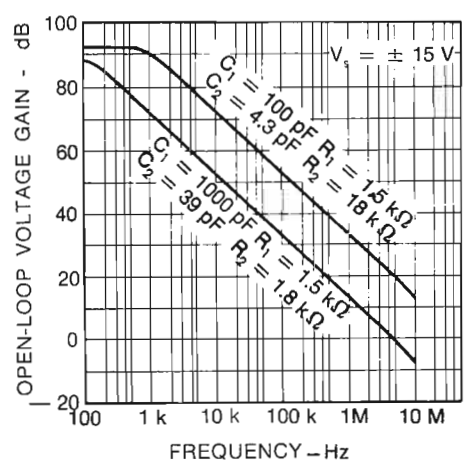


Fig. 5.26 - Frequency Compensation Circuit for Wider Band and Open Loop Voltage Response

Fig. 5.27 shows a unity-gain inverter amplifier designed according to these principles: the capacitor C_f = 3 pF compensates for the effect of input capacitance. It feaures a bandwidth of about 2 MHz, a full-power response up to 20 KHz and slewing rate of 1.5 V/μsec.

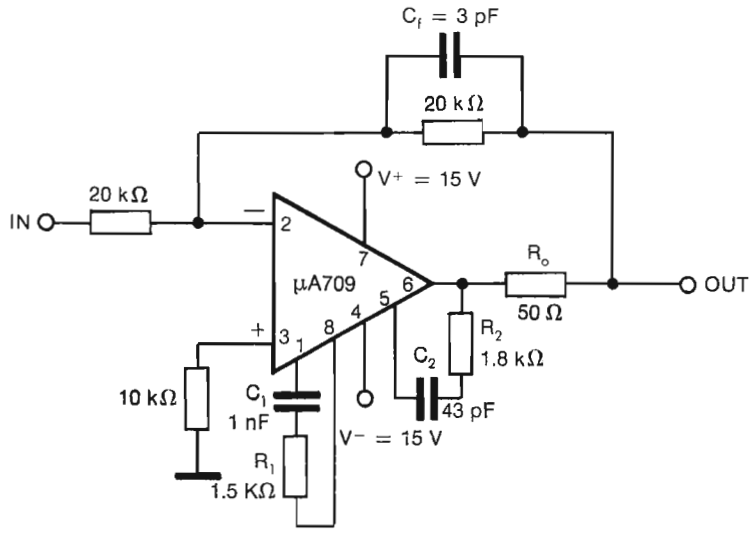


Fig. 5.27 - Wideband Unity Gain Inverting Amplifier

6. NOISE

6.1 GENERAL

6.1.1 Introduction

The precise meaning of noise has various interpretations but, as far as the electronic engineer is concerned, it may considered to be any form of unwanted signal present in a circuit. The ultimate aim of this section is to provide sufficient information in order that the quantity of noise present at the point of interest in a circuit can be calculated, together with information as to the relative amount contributed by the presence of the integrated active device. Before this can be done, however, it is necessary that the engineer be familiar with the terms commonly used when discussing noise. He should also be aware of the relative significance of the parameters these terms describe and be given an idea of the way in which they may be measured. With a clear understanding of these things, combined with an idea of the mechanism by which noise is generated within an integrated circuit device, the engineer should be in a position to design in order to minimise the effect of noise.

In the initial parts of this section, the noise characteristics of an amplifier are discussed in terms of the generalised theory concerning a four-pole network. It is then shown how the integrated noise values can be obtained from the characteristics of the single frequency noise voltage and noise current parameters. Results are given in graphical form, from which an estimate can be made of the noise figure of an amplifier having an idealized frequency response curve closely approximating those often met in practical applications.

6.1.2 Noise Terminology

In order to provide a measure of the effect of noise in a circuit, the concept of a signal-to-noise ratio has been developed.

Signal-to-Noise Ratio (S.N.R.) is defined as the ratio of the available signal power to the noise power present at a specific point in the circuit, i.e.,

$$\text{S.N.R.} = \frac{P_s}{P_n} = 10 \log_{10} \frac{P_s}{P_n} \qquad \ldots\ldots\ldots\ldots (1)$$

(where S.N.R. is expressed in dB).

In order to examine the effects of introducing a noise generating active network (e.g. an amplifier) into a circuit, it is necessary to define further terms, thus:

Noise Factor (F) defined as the input-to-noise ratio divided by the output signal-to-noise ratio. Alternatively, it may be defined as the ratio of the noise power output to noise power input divided by the network power gain.

$$F = \frac{P_{si}}{P_{ni}} \frac{P_{no}}{P_{so}} = \frac{P_{no}}{P_{ni}} \cdot \frac{1}{G} \qquad \ldots\ldots\ldots (2)$$

Where P_{si} = Signal input power
P_{so} = Signal output power
P_{ni} = Noise input power
P_{no} = Noise output power
G = Power gain

It may be seen that the noise factor gives a figure of merit for the active network and a measure of its contribution to the overall signal-to-noise ratio since it is independent of the signal-to-noise ratio present at the input.

Noise Figure (NF) is defined as the logarithm of the noise factor F expressed in dB i.e.:

$$NF = 10 \log_{10} F \qquad \ldots\ldots\ldots\ldots (3)$$

Note: Inconsistency exists over the usage of these expressions in literature on noise but, for the purpose of this Section, the above definitions will be adhered to.

The physical phenomena involving the random movement of free electrons in a conductor due to thermal agitation, was originally offered by Johnson as an explanation for the excess noise present in his valve amplifier circuits.

The resultant sum of electron movement within a conductor is not necessarily zero at any one instant, although the integrated sum averages to zero with time, in the absence of external influences (e.g. thermal or electrical gradients). The current resulting from the electron charge movement develops a voltage across the resistance of the conductor. The important characteristics of the voltage or « noise » is that its energy level has a constant distribution with respect to the frequency spectrum.

Nyquist showed that the mean squared noise voltage is given by:

$$\overline{e^2_r} = 4KTB_{eq}R \qquad \ldots\ldots\ldots\ldots\ldots\ldots (4)$$

K = Boltzmann's Constant = $1.38 \cdot 10^{-23}$ joules per degree Kelvin

T = Temperature of conductor in degrees Kelvin
B_{eq} = Effective bandwidth of voltage measuring equipment
R = Resistance of conductor in ohms

From this relationship, we can obtain the concept of the **Equivalent Noise Resistance. (R_{eq}).**

By choosing an arbitrary temperature of 27°C (300° Kelvin), an expression for the equivalent noise resistance is obtained from:

$$\overline{e^2_r} = 1.65 \cdot 10^{-20} B_{eq} R \qquad \ldots\ldots\ldots\ldots (5)$$

Thus any noise source can be replaced by an equivalent noise resistor (R_{eq}) when:

$$R_{eq} = \frac{\overline{e^2_r}}{B_{eq}} \cdot \frac{10^{20}}{1.65} \Omega \qquad \ldots\ldots\ldots\ldots\ldots (6)$$

It is assumed that the noise source to be replaced has an even distribution of energy with respect to frequency over the bandwith considered. This type of characteristic, as exhibited by the perfect theoretical resistor, is often referred to as « White Noise », based on the parallel concept of white light resulting from a combination of light energy from all of the visible spectrum. It should be pointed out that this would have a constant spectral density based on energy per unit wavelength bandwidth, whilst so-called white noise is defined as having constant energy per unit frequency bandwidth. Since the relationship between frequency and wavelength is given by:

$$F = \frac{v}{\lambda} \qquad \ldots\ldots\ldots\ldots\ldots (7)$$

where v is the velocity of propagation, therefore

$$df = \frac{v}{\lambda^2} \Delta \lambda \qquad \ldots\ldots\ldots\ldots\ldots (8)$$

This demonstrates that equal increments of wavelength corresponds to decreasing increments of frequency as the wavelength increases.

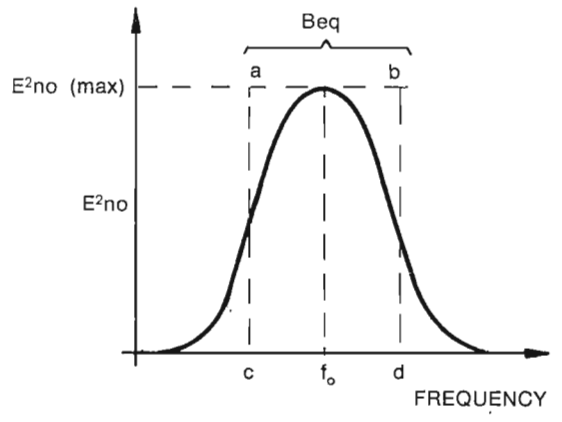


Fig. 6.1 - Amplifier Response Curve and Equivalent Bandwidth

Another useful term to define is **Equivalent Noise Bandwidth (B_{eq}).** This is the width of an ideal bandpass filter transmittance which has an absolute value equal to the maximum absolute of the transmittance function under consideration and which delivers the same mean-square total output voltage (or current) from a white noise source.

As an example, Fig. 6.1 might represent the output response of an amplifier stage having a white noise input. Mean-square output voltage E^2_{no} is plotted against frequency. The area under the curve representing the total mean-squared output voltage is equal to the noise bandwidth multiplied by the maximum mean squared output voltage. This is expressed mathematically by:

$$B_{eq} = \frac{1}{E^2_{no(max)}} \cdot \int_{f=\infty}^{f=0} E^2_{no}\, df \qquad \ldots\ldots\ldots (9)$$

Associated with any noise voltage e_n from a source of resistance R_s is the concept of **Available Noise Power.** This represents the maximum noise power that could be delivered to a load resistance R_L where Fig. 6.2 (a) represents the equivalent circuit. For maximum power transfer, $R_L = R_s$.

If the noise source is a resistance R_s then maximum power available is given by:

$$P_{an} = \left(\frac{e_r}{2}\right)^2 \cdot \frac{1}{R_s} = \frac{\overline{e^2_r}}{4R_s} \qquad \ldots\ldots\ldots (10)$$

But, from Equaton (4) we have: $\overline{e^2_r} = 4KTB_{eq}R_s$
Therefore,

$$P_{an} = KTB_{eq} \qquad \ldots\ldots\ldots\ldots\ldots (11)$$

It will be noted that the available noise power associated with the resistance is independent of the magnitude of the resistance generating the noise and depends only upon the bandwidth and absolute temperature. Further, it should be noted that this power is not practically realizable since the resistance R_L will also be at some finite temperature and, therefore, will also have a noise voltage associated with it.

It is useful to consider a signal e_s in series with its source resistance R_s generating a thermal noise voltage e_r, see Fig. (6.2 (b). From Equation (1), it can be shown that the signal-to-noise ratio is given by:

$$S.N.R. = \frac{e^2_s}{\overline{e^2_r}} = \frac{e^2_s}{4KTRB_{eq}} \qquad \ldots\ldots (12)$$

From Equation (11), this can be re-written as:

$$S.N.R. = \frac{\text{Available Signal Power}}{\text{Available Noise Power}} = \frac{P_{as}}{P_{an}} \qquad \ldots (13)$$

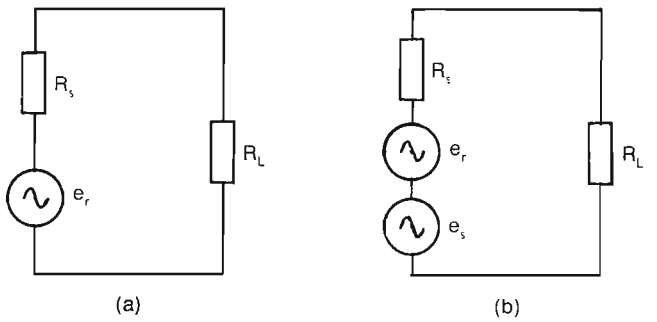


Fig. 6.2 - Equivalent Circuit for Maximum Available Noise Power

Hence, the available signal power is given by:

$$P_{as} = \frac{e^2_s}{4R_s} \qquad \text{..... (14)}$$

(where $R_s = R_L$)

Thus although the maximum S.N.R. would be given by the condition R_L = infinity, when the circuit is matched for maximum signal power transfer, the noise across the load terminals has increased by the ratio $\frac{1}{\sqrt{2}}$ since R_L itself contributes to the noise voltage (assuming $R_L = R_s$ and that both the resistors are at the same temperature).

It can be seen that the signal-to-noise ratio has been reduced by a factor of 0.5. The addition of a matching load resistor, therefore, degrades the S.N.R. by 3 dB.

6.1.3 An Amplifier considered as a Four-pole Network

Network theory shows that, in general, an amplifier may be represented as a four-pole (quadripole) network. More specifically a differential input, single-ended output amplfier could be described as a two-port, four-pole network.

The noise characteristics of this type of network may be defined in terms of an equivalent noiseless four-pole network combined with one current and one voltage noise generator connected across the input, see Fig. 6.3. The resultant, input referred, noise parameters are therefore those of a noise voltage generator with the input to the network short-circuit, and a noise current generator with the input open-circuit. These two quanties are usually in terms of the root-mean-squared values per cycle.

$\sqrt{\overline{e^2_n}}$ and $\sqrt{\overline{i^2_n}}$

(i.e. typically microvolts or picoamps per cycle). The values $e^2_n\Delta(f)$ and $i^2_n\Delta(f)$ would represent their respective contributions to the total noise over a frequency inteval Δ f. By measurement of these parameters, the noise characteristics of an amplifier represented as a four-pole network are defined in terms of:

$$e^2_n = e^2_n\ (f)$$
$$i^2_n = i^2_n\ (f) \qquad \text{..... (15)}$$

It is usual to find, for an amplifier manufactured in integrated circuit form, that when $\overline{e^2_n}$ and $\overline{i^2_n}$ are plotted as a function of frequency, both exhibit an energy spectrum proportional to 1/f at low frequencies (attributable to « flicker noise »).

It is convenient to separate the noise parameters into two components, one having an energy per frequency spectrum that is approximately constant and for which the relationship holds good to high frequencies (equivalent to « shot noise ») and another component which predominates at low frequency, having an energy density spectrum proportional to 1/f. Equation (15) may be written in the form:

$$\overline{e^2_n} = \overline{e^2_{ns}} + \overline{e^2_{nf1}}\,\frac{f_1}{f}$$
$$\overline{i^2_n} = \overline{i^2_{ns}} + \overline{i^2_{nf1}}\,\frac{f_1}{f} \qquad \text{..... (16)}$$

Where $\overline{e^2_{ns}}$ $\overline{e^2_{nf}}$ and $\overline{i^2_{ns}}$ $\overline{i^2_{nf}}$ are able to be measured experimentally up to a sufficiently high frequency for $\overline{e^2_n} \approx \overline{e^2_{ns}}$ and $\overline{i^2_n} \approx \overline{i^2_{ns}}$ and down to a sufficiently low frequency such that $\overline{e^2_n} \approx \overline{e^2_{nf}}$ and $\overline{i^2_n} \approx \overline{i^2_{nf}}$

The Noise Factor (F) and hence Noise Figure (N.F.) for the four-pole network (or amplifier) is determined from the relationships shown in equations (2) and (3) of Section 6.1.2. The relationship

between noise factor and the noise parameters expressed in terms of voltage and current is given by:

$$F = \left[\frac{\overline{e^2_n}}{R_S} + \overline{i^2_n}R_S + \overline{\gamma e_n \cdot i_n} + \frac{e^2_r}{R_S}\right] \Big/ \frac{\overline{e^2_r}}{R_S} \quad \ldots\ldots\ (17)$$

Where $\frac{\overline{e^2_r}}{R_s}$ is the thermal noise power due to the source resistance (R_s) and is evaluated from Equation (4) of Section 6.1.2. γ is the correlation factor between the two noise generators and is given by:

$$\gamma = \frac{\overline{e_n i_n}}{\overline{e_n} \cdot \overline{i_n}}$$

As a first approximation it can be assumed that the two generators act independently and no correlation exists (i.e. $\gamma = 0$), although this is strictly true only for « shot noise ». Therefore Equation (17) may be simplified and written as:

$$F = 1 + \frac{\overline{e^2_n} + \overline{i^2_n}R^2_S}{4\,KTR_S} \quad \ldots\ldots\ldots\ (18)$$

The Noise Figure (see Equation (3), Section 6.1.2) is given by:

$$N.F. = 10 \log_{10} \left[1 + \frac{\overline{e^2_n} + \overline{i^2_n}R^2_S}{4\,KTR_S}\right] \quad \ldots\ldots\ldots\ (19)$$

The opimum value of source resistance $R_{s(opt)}$ to correspond with the minimum noise figure ($N.F._{(min)}$) may be obtained by the use of standard algebraic manipulation on Equation (19) involving differentiation and equating to zero. This gives the result:

$$R_{S(opt)} = \sqrt{\frac{\overline{e^2_n}}{\overline{i^2_n}}}$$

Substitution for $R_{S(opt)}$ in Equation (19) gives:

$$N.F._{(min)} = 10 \log_{10} \left[1 + \frac{\overline{e^2_n i^2_n}}{2\,KT}\right] \quad \ldots\ldots\ldots\ldots\ (20)$$

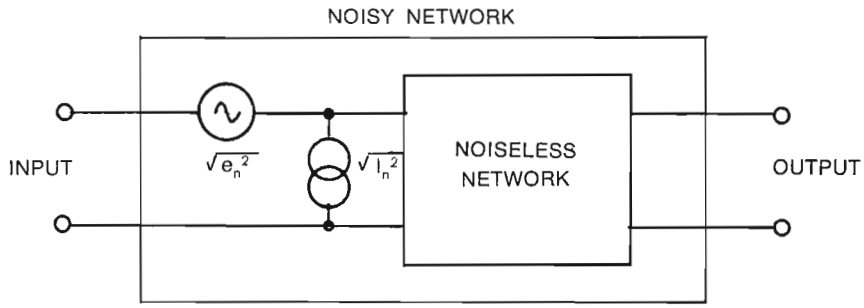


Fig. 6.3 - Noisy Network is Characterised by an Equivalent Noiseless Network plus Noise Current and Noise Voltage Generators

If the source presents a complex impedance (Z_s) then the expression $\overline{i^2_n}R^2_s$ in Equations (17) and (18) is replaced by $\overline{i^2_n}|Z_s|^2$ If it is purely reactive (X_s) then, with reference to Section 6.1.2, it may be more convenient to express it as:

$$S.N.R. = \frac{e^2_s}{\overline{e^2_{n(total)}}} = \frac{e^2_s}{\overline{e^2_n} + \overline{i^2_n}\,|X_s|^2}$$

6.1.4 Evaluation of the Integrated Noise Factor for a Four-pole Network

The total noise associated with a four-pole network (and therefore an amplifier) depends not only on its own noise characteristics expressed in terms of $\overline{e^2_n}$ and $\overline{i^2_n}$ as shown above, but also on the source impedance and shape of the overall frequency response.

In order to evaluate the total noise, the integrated noise voltage and current (e_N and i_N) must be calculated from the relationships:

$$e^2_N = \int_{f=0}^{f=\infty} \overline{e^2_n}(f)\, A^2_r(f)\, df \quad \ldots\ldots\ (21)$$

$$i_N{}^2|Z_S|^2 = \int_{f=0}^{f=\infty} \overline{i^2_n}(f)|Z_S(f)|^2\, A^2_r(f)\, df \quad \ldots\ldots\ldots\ldots\ (22)$$

Where A_r (f) is the relative gain as a function of frequency as given by the expression (Fig. 6.1 of Section 6.1.2):

$$A_r(f) = \frac{A(f)}{A(f_o)}$$

For a purely resistive load, Equation (22) simplifies to:

$$i^2_N R^2_S = R^2_S \int_{f=0}^{f=\infty} \overline{i^2_n}(f)\, A^2_r(f)\, df \qquad \ldots\ldots\ldots (23)$$

The integrated thermal noise voltage (e_R) which has a flat energy spectrum with respect to frequency, is given by:

$$e^2_R = e^2_r \int_{f=0}^{f=\infty} A^2_r(f)\, df = e^2 B_{eq} \qquad \ldots\ldots\ldots\ldots (24)$$

Where B_{eq} is the equivalent noise bandwidth (6.1.2 Equation (9) and Fig. 6.1).

Having calculated the values of e^2_N, i^2_N, and e^2_R as above, the integrated noise factor, noise figure and optimum source resistance are obtained by substituting for $\overline{e^2_n}$, $\overline{i^2_n}$ and e^2_r in Equations (17) to (20).

Analytical solutions for Equations (21) to (24) may prove difficult to obtain due to the integration involved and it is often more convenient to carry out graphical integration. If, however, the network noise and frequency response characteristics can be approximated to fit idealized curves formed from straight lines, then expressions in Equations (21) to (24) can be suitably simplified, making analytical solutions practical.

A frequency response common to many applications is where there is constant gain from low frequency up to a higher « cut-off » frequency (f_2) at which the gain reduces at a rate of 6 dB per octave (i.e. 20 dB per decade). Fig. 6.4 shows the relative gain response with the origin at a frequency $f_1 = 1$ Hz. Using this approximation, the error due to « shot noise » and « thermal noise » components is negligible if:

$$f_2 \gg f_1$$

The characteristics of the « flicker noise » component is not known at very low frequencies, but it is thought that the 1/f relationship does not continue indefinitely. In any case, extension of the lower frequency limit would significantly increase the time needed for making each noise measurement and since the commercially-available measuring equipment does not usually have a passband lower than a few cycles per second, specifying a frequency lower than 1 Hz would have little practical significance.

It may be shown that for the frequency response in Fig. 6.4, Equations (21), (23) and (24) may be approximated to:

$$e^2_N \approx e^2_{ns} \frac{\pi}{2} f_2 + e^2_{nf1} \cdot f_1 \log_e \frac{f_2}{f_1}$$

$$i^2_N \approx i^2_{ns} \frac{\pi}{2} f_2 + i^2_{nf1} \cdot f_1 \log_e \frac{f_2}{f_1}$$

$$e^2_R \approx e^2_r \frac{\pi}{2} f_2 \qquad \ldots\ldots\ldots (25)$$

These expressions facilitate rapid calculation of the integrated Noise Factor, and hence Noise Figure, with various values of source resistance and cut-off frequency (f_2).

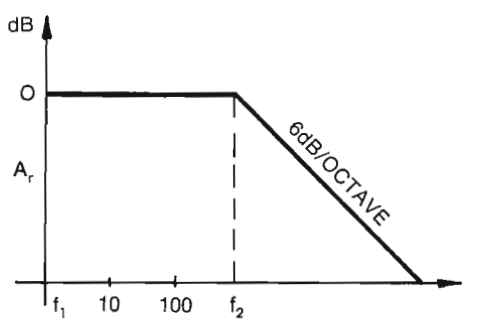


Fig. 6.4 - Frequency Response Used for Noise Computation

6.1.5 Noise Voltage and Current Measurement Methods

The overall noise figure for four-pole networks connected in series (e.g. an amplifier with several stages in cascade) is given by:

$$N.F. = 10 \log_{10} \left[F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \right] \ldots\ldots (26)$$

Where F_1, F_2 and F_3 are the noise factor values for the first, second and third stages, etc, and G_1, G_2 are the relative power gains under optimum matched conditions. It can be seen that if gain of the first stage is sufficiently high, the overall N.F. is dictated primarily by the characteristics of the first stage, It may also be seen that if the power gain falls off at

high frequencies, an increase in the N.F. value will result.

The relationship shown in Equation (26) is useful since it enables an additional amplifier to be used at the output of the one under test for the purpose of increasing the output signal to conveniently large values for the noise measurements to be taken. if the above conditions are satisfiied, then this amplifier (sometimes called a post-amplifier) need not have an especially low-noise performance before its contribution to the total system noise can be neglected.

A typical circuit for the measument of equivalent noise voltage is shown in Fig. 6.5. This consists of a constant impedance input attenuator, the four-pole network under test, a post amplifier (such as a μA702A) and a narrow bandpass filter. It is assumed that the energy density spectrum of the noise over this narrow frequency bandwidth is constant.

The effectice source resistance (R_S) must be sufficiently small so that the thermal noise voltage and noise current contribution is negligible. This will then approximate to the condition of a short-circuit input. This will be realized if R_s is chosen such that:

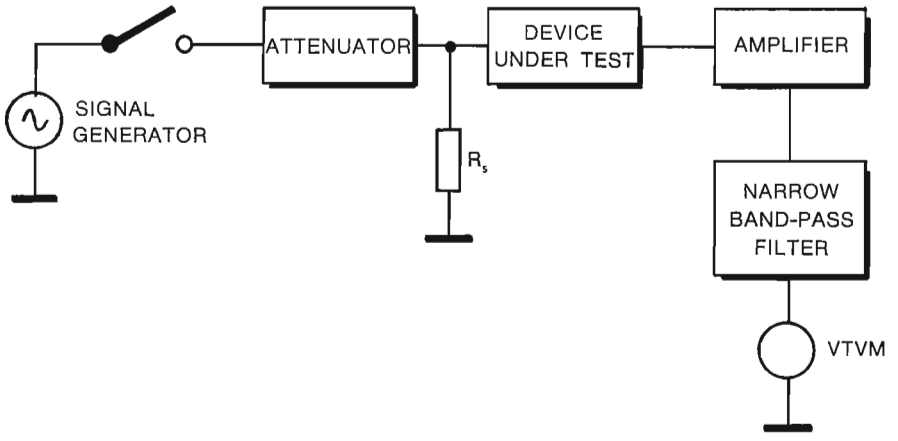


Fig. 6.5 - This Setup is Used to Measure Equivalent Noise Voltage

$$R_s \ll \sqrt{\frac{\overline{e^2_n}}{\overline{i^2_n}}} = R_{s(opt)}$$

The measuring procedure is as follows:

1. With signal generator disconnected, the noise voltage ($e_{N(out)}$) at the output is measured by means of the VTVM.
2. The signal generator is connected and adjusted with the aid of the attenuator to give an output level ($e_{T(out)}$) at least 20 dB or 40 dB above that of the noise alone. The input signal (e_{in}) to the four-pole network from the signal generator is determined, knowing the degree of attenuation and the generator output signal level.
3. The original input-referred noise voltage (e_N) is calculated using the relationship:

$$e_N = e_{N(out)} \frac{e_{in}}{e_{T(out)}} \qquad \ldots\ldots\ldots\ldots (27)$$

Where the ratio $\frac{e_{T(out)}}{e_{in}}$ closely approximates to the voltage gain of the amplifier under investigation.

If the filter has an equivalent bandwidth of 1 Hz, Equation (27) gives the single frequency (sometimes called « spot ») noise voltage (e_n) directly. Otherwise this may be calculated from the formula:

$$e^2_n = \frac{e^2_N}{B_{eq}}$$

Measurement of the equivalent noise current (i^2_n) is carried out by means of a similar type of circuit, in which a high value resistance (R_S) is inserted in series with the input attenuator as shown in Fig. 6.6. To ensure that the measuring conditions closely approximate that of an open-circuit input and that the contribution of the thermal noise voltage to the total can be ignored, the value of R_S must be such that:

$$R_s \gg \sqrt{\frac{\overline{e^2_n}}{\overline{i^2_n}}} = R_{s(opt)}$$

$$\overline{i^2_n} \gg \frac{4KT}{R_s}$$

The measurement procedure for obtaining the noise current is similar to that for the noise voltage.

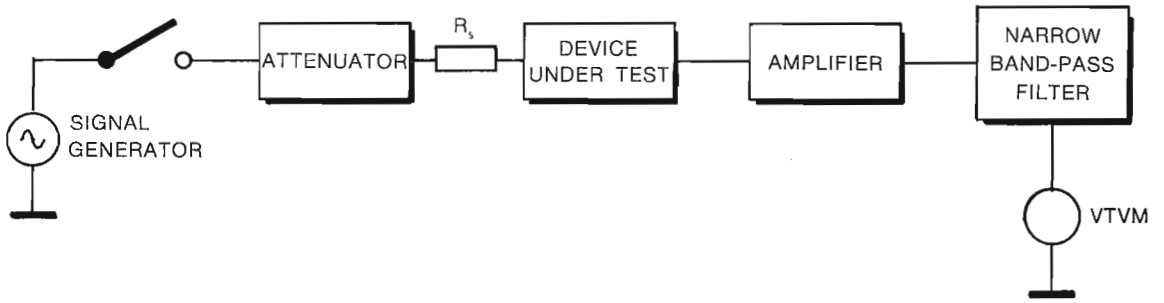


Fig. 6.6 - This Setup is Used to Measure Equivalent Noise Current

6.2 NOISE CHARACTERISTICS OF THE μA702A

6.2.1 Noise Characteristics as a Function of Frequency

Section 6.1 describes how the noise characteristics of a four-pole network can be defined in terms of the parameters of an equivalent noise voltage and noise current generator, each of which is frequency dependent. Figs. 6.7 and 6.8 show these typical characteristics for the μA702A, over a range from 10 Hz to 1 MHz expressed in terms of V^2 per cycle and A^2 per cycle.

It may be seen from these graphs that at lower frequencies a 1/f (flicker noise) relationship predominates. As the frequency is increased the curves level to an approximately constant value of noise energy due to the « shot noise » only. The crossover frequency, at which the separate noise components contribute equally to the total noise, is relatively low for the noise voltage (5 KHz) and considerably higher for the noise current (80 KHz).

By comparing the noise voltage values with that contributed by the noise current generator developed across the source resistance (R_s) it can be seen that if $R_s < 200\ \Omega$ the noise current contribution can be ignored and if $R_s \geq 20\ k\Omega$ then the noise current contribution predominates and the noise voltage can be neglected. Fig. 6.9 shows a graph of noise figure plotted against frequency for various values of source resistance. It can be seen that as R_s increases, so does the bandwidth over which the 1/f relationship predominates.

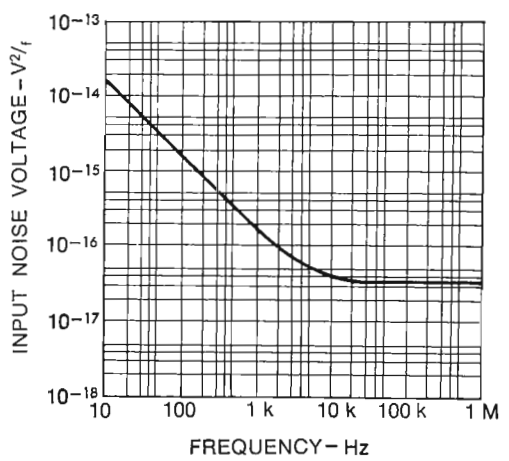


Fig. 6.7 - Typical Input Referred Noise Voltage of the μA702A for one Cycle Bandwidth as a Function of Frequency

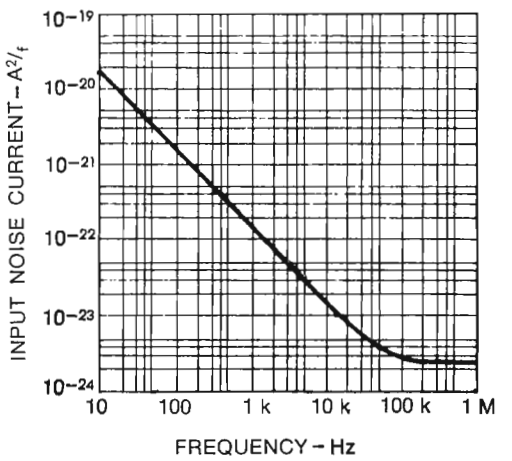


Fig. 6.8 - Typical Input Referred Noise Current of the μA702A for one Cycle Bandwidth as a Function of Frequency

6.2.2 Integrated Noise Characteristics of the μA702A

The noise contributed by an amplifier within a system depends on the appropriate noise parameters, the source resistance and effective pass-

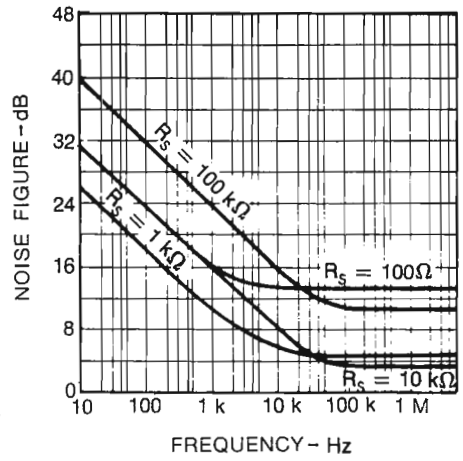


Fig. 6.9 - Noise Figure (NF) Versus Frequency for the μA702A

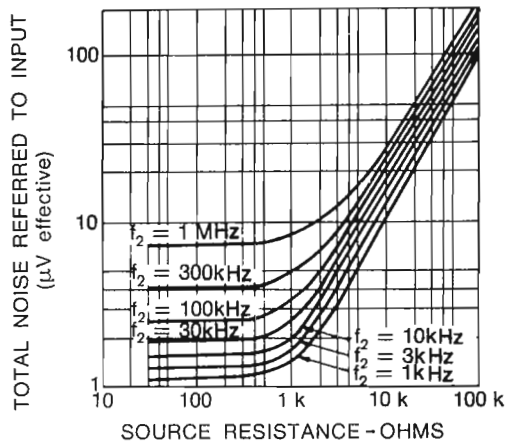


Fig. 6.10 - Typical Total Input Referred Noise of the μA702A as a Fuction of Resistance and Cut-off Frequency (f_2)

band. In Section 6.1.4 it was shown that it is possible, knowing the voltage and current noise parameters as a function of frequency, to obtain the integrated noise characteristics by means of Equations (21) to (24). A method of solving these equations by means of graphical integration is shown in the following example.

An amplifier fed from a source resistance of 1 kΩ is specified having an upper and lower cut-off frequency at 10 KHz and 1 KHz respectively. The frequency response, determined by reactive elements or by a following filter, falls off with a slope of 6 dB per octave (20 dB per decade) at the high-frequency end and at 12 dB per octave at low frequencies. The noise voltage per cycle over the bandwidth, $e^2_n(f)$ $A^2_r(f)$ is found by multiplying the value of the curve for $\overline{e^2_n}$ by the square of the relative voltage gain. The effective noise current $i^2_n(f)$ $A^2_r(f)$ is obtained in a similar manner. These new values can be replotted on a linear frequency scale, having multiplied the effective noise current by the square of the source resistance to obtain the equivalent noise voltage contribution of the noise current developed across this resistance. The area enclosed by these two curves give the integrated noise value. In the above example the following values were obtained:

$$e^2_N = 5.7 \cdot 10^{-13} V^2 \qquad i^2_N R_S = 2.7 \cdot 10^{-13} V^2$$

To find the total noise present the contribution due to the effective thermal noise of the source resistance must be added to these values thus:

$$e_T = \sqrt{e^2_N + i_N{}^2 R^2_S + e^2_R} \qquad \ldots\ldots\ldots (1)$$

This method, although easy to apply is time-consuming and so, in Fig. 6.10, a graph is shown of the total noise voltage (e_T) for the μA702A plotted against source resistance using, as a basis for calculation, an amplifier having the idealized frequency response shown in Fig. 6.4 of Section 6.1.4 and where the cut-off frequency (f_2) varies from 1 KHz to 1 MHz. With the aid of the graph in Fig. 6.11 which shows the integrated thermal noise voltage (e_R) against source resistance for an approximately similar response curve and cut-off frequencies, the Noise Figure for this amplifier is obtained from the relationship:

$$N.F. = 20 \log_{10} \frac{e_T}{e_R} \qquad \ldots\ldots\ldots\ldots (2)$$

These calculations have been carried out and in Fig. 6.12 the noise figures are plotted against source resistance for various values of cut-off frequency. From this graph, it is possible to estimate rapidy the typical N.F. of a μA702A amplifier having a frequency response common to a good general, practical applications.

It can be seen that as the amplifier cut-off frequency increases, the optimum value of source resistance for which a minimum N.F. is obtained, increases from 1 kΩ to 3 kΩ. The minimum overall N.F. is obtained using a high value of cut-off frequency since, in this case, the additional effect of flicker noise has the least influence.

6.3 NOISE CHARACTERISTICS OF THE μA709

6.3.1 Noise Characteristics as a Function of Frequency

The best way to characterize the noise performance of an amplifier is to specify the equivalent input noise voltages and currents, as a function of frequency.

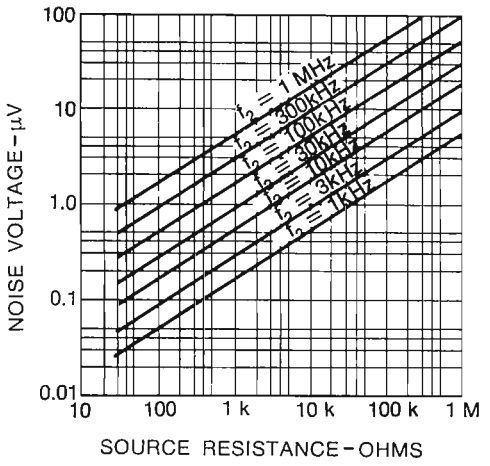


Fig. 6.11 - Thermal Noise Voltage Versus Resistance and Cut-off Frequency (f_2)

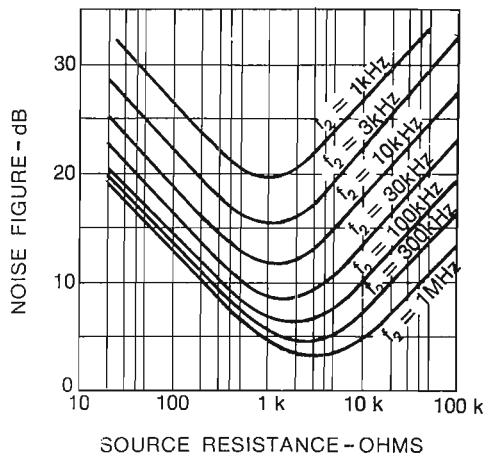


Fig. 6.12 - µA702A Noise Figure (NF) Versus Source Resistance and Cut-off Frequency (f_2) for the Idealised Frequency Response of Fig. 6.4.

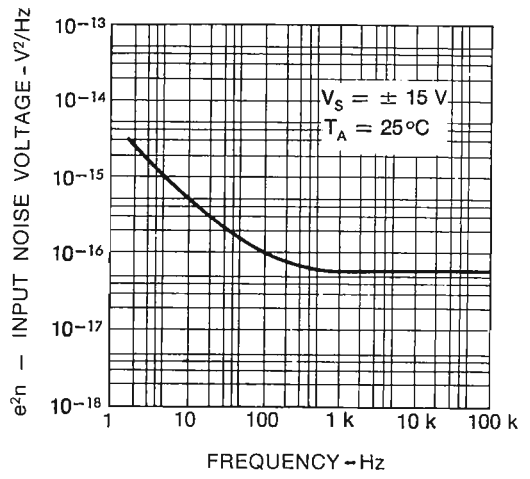


Fig. 6.13 - Typical Input Noise Voltage of the µA709 for one Cycle Bandwidth as a Function of Frequency

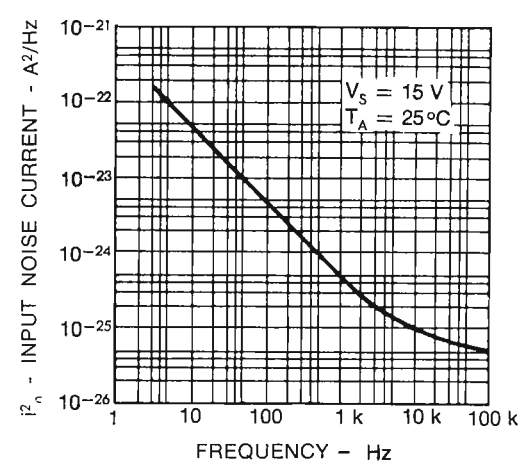


Fig. 6.14 - Typical Input Noise Current of the µA709 as a Function of Frequency

Fig. 6.13 and 6.14 show typcal values of e^2_n and i^2_n for the µA709 element versus frequency.

Examining these diagrams it is possible to distinguish a region (high frequency) having a flat power spectrum in which the shot noise prevails, and another region (low frequency) having a power spectrum proportion to 1/f in which the flicker noise predominates.

The frequency where the amount of the two noise components (shot and flicker) is equal to each other is very low for the noise voltage (95 Hz) while it is comparatively high for the noise current (10 KHz).

The noise current contribution is negligible for source resistors ≤3 kΩ while for high values of source resistors (≥200 kΩ) the contribution of noise voltages can be neglected.

Comparating the noise parameters of the µA702A with the µA709 shows how better are the noise characteristics of the latter element compared with the µA702A at low frequencies, and, moreover how the noise current is considerably lower. This is in accordance with fact that the µA709 input stage operates at a current level approximately ten times lower than that of the µA702A.

Fg. 6.15 indicates the characteristics (under equal noise figure conditions) as a function of frequency and source resistance.

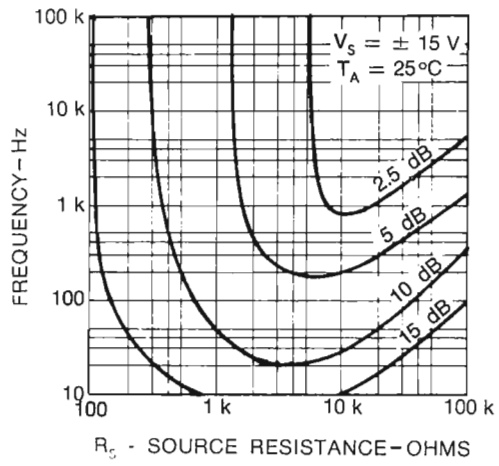


Fig. 6.15 - Typical Spot Noise Figure Contours Versus Source Resistance and Frequency

6.3.2 Integrated Noise Characteristics of the μA709

Once the source resistance and bandwidth are know it is possible (see Section 6.1) to calculate the integrated noise by application of the proper integration operations carried out graphically and analytically: this is done, having previously estimated the values of voltage and current noise squared as a function of frequency.

Fig. 6.16 shows the total noise voltage for a frequency response which has a constant gain from f_1 (1 Hz) to f_2 and then a decrease with a 20 dB/dec slope, as a function of the source resistances for different values of f_2.

From this characteristic it is possible to obtain, quickly, the total noise voltage of the μA709 (referred to the input) for most applications.

Finally, Fig. 6.17 shows typical values of the noise figure as a function of source resistance, for different values of cut-off frequency.

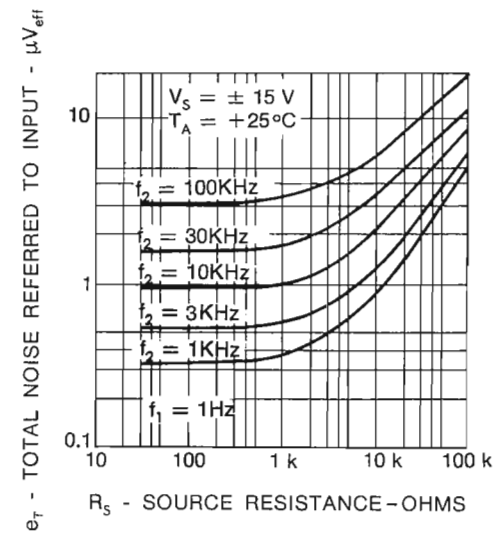


Fig. 6.16 - Typical Total Noise Referred to Input of μA709 as a Function of Source Resistance and Bandwidth

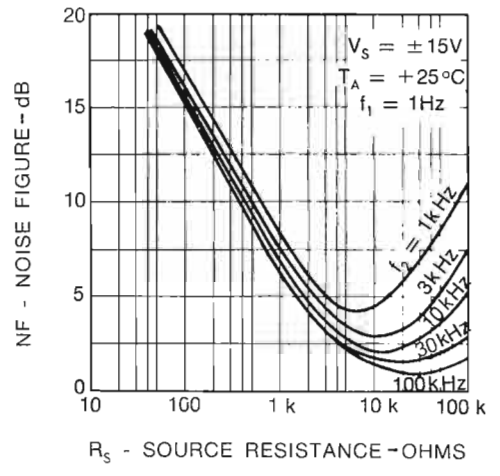


Fig. 6.17 - Typical Noise Figure of μA709 Versus Source Resistance and Bandwidth

From this graph it can be seen that the optimum value of source resistance is between 7 kΩ and 30 kΩ when the bandwidth increases, and the minimum value of noise figure decreases when the cut-off frequency is raised. In this case the influence of the flicker noise on the integrated noise value is lower.

When compared with the μA702A, the operational amplifier μA709 shows a higher optimum source resistance with better performance or a minimum value of noise figure.

7. POWER SUPPLIES

7.1 GENERAL

7.1.1 Introduction

The specification of suitable power supplies plays an important part in the design of systems employing integrated circuits. The cost of close tolerance supplies rises sharply with increased demands for stability, regulation, etc. It is therefore necessary to understand the implications for power supply parameters with regard to integrated circuit performance in order to avoid under-specifying and obtaining poor results, or over-specifying with resultant economic penalties.

It may be pointed out that the small inherent design of the monolithic integrated circuit family and resultant low-power consumption reduces the problems attached to providing high-stability supplies.

During the design stage of integrated circuits, special attention is paid to obtaining high power-supply fluctuation rejection (see Section 2.1). In that family of circuits where this is likely to be important (e.g., in D.C. amplifier applications), balanced differential pairs and a constant current source are generally employed.

7.1.2 Mandatory Characteristics

Before more closely examining the effects of power supply parameters, there are some general comments on desirable characteristics that are relevant to the majority of applications in which integrated circuits are used. Some of these comments may appear obvious, but catastrophic failure of devices has been caused by neglecting to observe what, in retrospect, are seen to be elementary precautions.

In common with other semiconductor devices, the PN junction within the monolithic integrated circuit exhibits reverse voltage breakdown characteristics. Because of this and due to certain dissipation considerations, maximum ratings for power supply voltages are given for each device type.

Exceeding these ratings, even for very small periods of time, may promote failures caused by, for example, avalanche breakdown.

Whether proprietary supplies or especially designed ones are to be employed, care must be taken to ensure that, at switch « on » or « off », transient over-voltages or even reversal of polarity does not occur. Similarly, with mains supply circuits, it is possible for break-through of transients from the raw supply to cause trouble. Minimal inter-winding capacitance and earth screening can help here.

Many stabilized power supplies which have excellent D.C. regulation prove to be unsuitable without modification if they have a high A.C. impedance. The very high open-loop gain such as is found in the μA702A, may result in positive feedback between the output and input via the power supplies, causing spurious oscillation. Since the amplifier still has potential gain at 30 MHz, decoupling must be effective up to this frequency. Satisfactory results are usually obtained using 0.01 μF to 0.1 μF capacitors connected from the positive and negative supply leads to earth, as close as is practical to the amplifier device itself, see Fig. 7.1. The possibility of inter-connector contact resistance and, at 30 MHz inductance in leads and « skin effect », make the above precautions advisable in many circuit configurations. Care should be taken in selecting suitable capacitors which are still effective at this frequency. In general,aluminium electrolytic types are not reccomended. Silver mica, certain metal foil, ceramic and solid tantalum types have proved to be suitable.

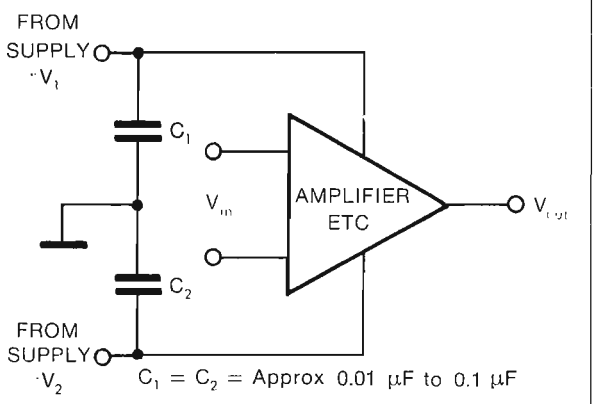


Fig. 7.1 - Decoupling of Power Supplies

Inter-action between devices, using common supply rails, has also to be considered, but in module constructions, such as on printed-circuit boards, it has usually proved sufficient to decouple at the end of each module bank. Conventional techniques for HF decoupling such as RC and LC circuits should be resorted to if further difficulties arise. If resistance is inserted between the supplies and device terminals, then D.C. level drift with increase in power demand must be calculated, taking these voltage variations into account.

During development work, at a breadboard stage and in servicing and fault-finding, demage to integrated circuits has been caused by using an electrically non-isolated soldering iron. Earth loops have been formed between poorly isolated power supplies, test equipment, etc. Safest results are usually obtained by adequately earthing all equipment and switching off the power supply before

using a soldering iron. It should be noted that the smoothing capacitor present at the output of some power supplies can hold sufficient energy to damage the input to devices up to minutes after switching off.

The design of the linear integrated circuit family is such that the sequence in which the power supplies are connected or disconnected are not critical. It is remotely possible, however, that associated input or output circuitry which was fed from the same supply could cause some damaging transient or leave the integrated circuit in a latched-up or saturated state if a certain switching sequence was not adhered to.

SGS